EPSON
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S1D15705 Series
Technical Manual

SEIKO EPSON CORPORATION

Rev.3.2

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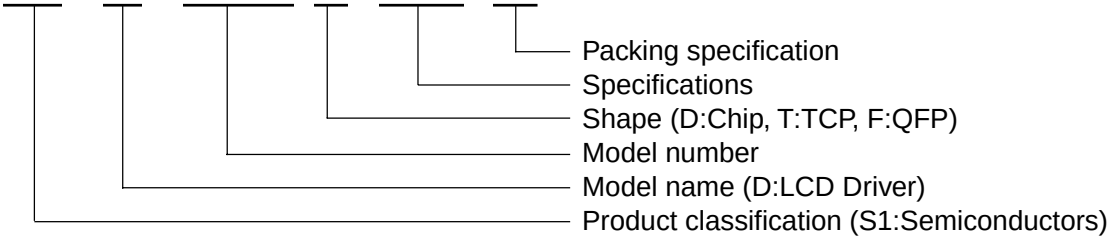
Configuration of product number

●DEVICES

S1 D 15705 D 00B0 00



Contents

1. DESCRIPTION

The S1D15705 series is a 1-chip dot matrix liquid crystal driver that can be connected to the bus of a microcomputer. It stores the 8-bit parallel or serial display data sent from the microcomputer in the built-in display data RAM and generates liquid crystal drive signals independently of the microcomputer. Since it incorporates 65 × 200 bits of the display data RAM and the one-dot pixel of the liquid crystal panel and one bit of the built-in RAM have a one-to-one correspondence, it enables display with the high degree of freedom.

The S1D15705 series incorporates 65 circuits of the common output and 168 circuits of the segment output and can display 65 × 168 dots (capable of displaying 10 columns × 4 rows of a 16 × 16 dot kanji font) using the single chip. The S1D15707 Series incorporates 33 circuits of the common output and 200 circuits of the segment output and can display 33 × 200 dots (capable of displaying 12 columns × 2 rows of a 16 × 16 dot kanji font). The S1D15708 series incorporates 17 circuits of the common output and 200 circuits of the segment output and can display 17 × 200 dots (capable of displaying 12 columns × 1 rows of a 16 × 16 dot kanji font). It can also expand the display capacity by using the two chips for the master and slave configuration.

Incorporating an analog temperature sensor circuit, the S1D15705∗10∗∗ can be used to constitute a system to provide optimum LCD contrast throughout a wide temperature range without need for use of supplementary parts such as the thermistor, under controls of a microcomputer.

Since the read/write operation of the display data RAM does not require external operation clocks, the S1D15705 series can be operated with the minimum current consumption. Since it also incorporates a liquid crystal drive power supply with low current consumption, liquid crystal drive power supply voltage adjusting resistor, and display clock CR oscillator circuit, it can provide a display system for high performance handy equipment with the minimum current consumption and the minimum parts configuration.

2. FEATURES

- Direct display of RAM data using the display data RAM
  RAM bit data "1" .... goes on.
  "0" .... goes off (at display normal rotation).
- RAM capacity
  65 × 200 = 13,000 bits
- Liquid crystal drive circuit
  The S1D15705 Series
  65 circuits for the common output and 168 circuits for the segment output
  The S1D15707 Series
  33 circuits for the common output and 200 circuits for the segment output
  The S1D15708 Series
  17 circuits for the common output and 200 circuits for the segment output
- High-speed 8-bit MPU interface (Both the 80 and 68 series MUPs can directly be connected.)/serial interface enabled
- Abundant command functions
  Display Data Read/Write, Display ON/OFF, Display Normal Rotation/Reversal, Page Address Set, Display Start Line Set, column address set, Status Read, Power Supply Save Display All Lighting ON/OFF, LCD Bias Set, Read Modify Write, Segment Driver Direction Select, Electronic Control, V_5 Voltage Adjusting Built-in Resistance Ratio Set, Static Indicator, n Line Alternating Current Reversal Drive, Common Output State Selection, and Built-in Oscillator Circuit ON
- Built-in static drive circuit for indicators (One set, blinking speed variable)
- Built-in power supply circuit for low power supply liquid crystal drive
  Booster circuit (Boosting magnification - double, triple, quadruple, boosting reference power supply external input enabled)
- 3% high accuracy alternating current voltage adjusting circuit (Temperature gradient: –0.05%/°C)
  Built-in V_5 voltage adjusting resistor, built-in V_1 to V4 voltage generation split resistors, built-in electronic control function, and voltage follower
- Built-in CR oscillator circuit (external clock input enabled)
- Ultra-low power consumption
- Built-in temperature sensor circuit (S1D15705D10B∗)
- Power supplies
  Logic power supply: $V_{DD} – V_{SS}$ = 2.4 to 3.6 V
  (S1D15705∗03∗∗, S1D15707∗03∗∗)
  $V_{DD} – V_{SS}$ = 3.6 to 5.5 V
  (S1D15705∗00∗∗, S1D15707∗00∗∗, S1D15708∗00∗∗)
  Boosting reference power supply: $V_{DD} – V_{SS}$ = 1.8 to 6.0 V
  Liquid crystal drive power supply: $V_5 – V_{DD}$ = –4.5 to –18.0 V (S1D15705∗∗∗∗∗) /–4.5 V to –16.0 V (S1D15707∗∗∗∗∗)/–4.5 V to –10.0 (S1D15708∗∗∗∗∗)
- Wide operating temperature range –40 to 85°C
- CMOS process
- Shipping form Bare chip, TCP
- No light-resistant and radiation-resistant design are provided.

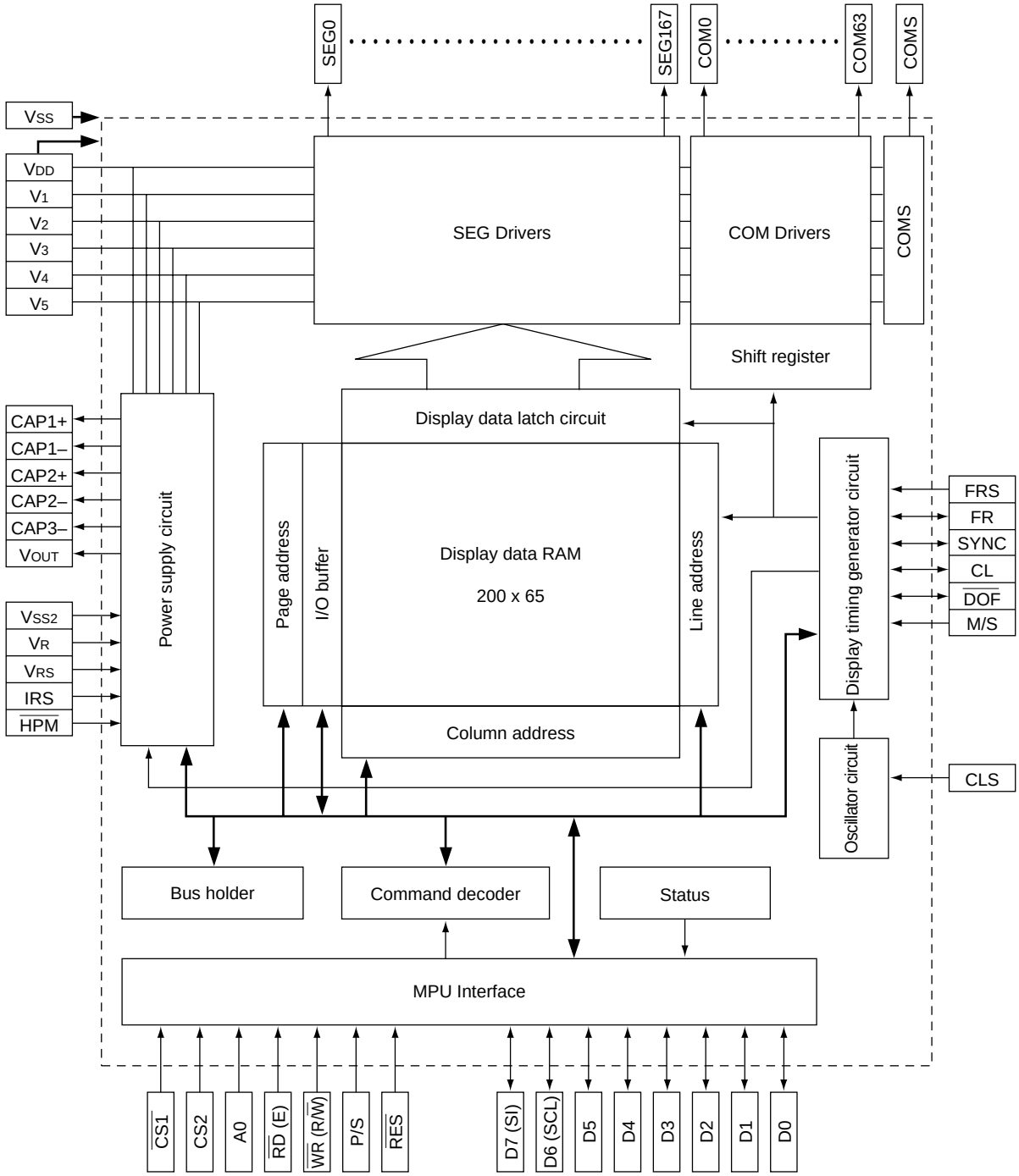
Series specification

Product name	Voltage [V]	Duty	Bias	SEG Dr	COM Dr	V_{REG} temperature gradient	Shipping form
S1D15705D00B*	–3.6 to –5.5	1/65	1/9, 1/7	168	65	–0.05%/°C	Bare chip
S1D15705D10B*	–3.6 to –5.5	1/65	1/9, 1/7	168	65	–0.05%/°C	Bare chip
S1D15705D03B*	–2.4 to –3.6	1/65	1/9, 1/7	168	65	–0.05%/°C	Bare chip
S1D15705T00A*	–3.6 to –5.5	1/65	1/9, 1/7	168	65	–0.05%/°C	TCP
S1D15705T03A*	–2.4 to –3.6	1/65	1/9, 1/7	168	65	–0.05%/°C	TCP
S1D15707D00B*	–3.6 to –5.5	1/33	1/6, 1/5	200	33	–0.05%/°C	Bare chip
S1D15707D03B*	–2.4 to –3.6	1/33	1/6, 1/5	200	33	–0.05%/°C	Bare chip
S1D15707T00**	–3.6 to –5.5	1/33	1/6, 1/5	200	33	–0.05%/°C	TCP
S1D15707T03**	–2.4 to –3.6	1/33	1/6, 1/5	200	33	–0.05%/°C	TCP
S1D15708D00B*	–3.6 to –5.5	1/17	1/6, 1/5	200	17	–0.05%/°C	Bare chip

Specifications for circuits other than the temperature sensor circuit are the same as those of the S1D15705D00B.

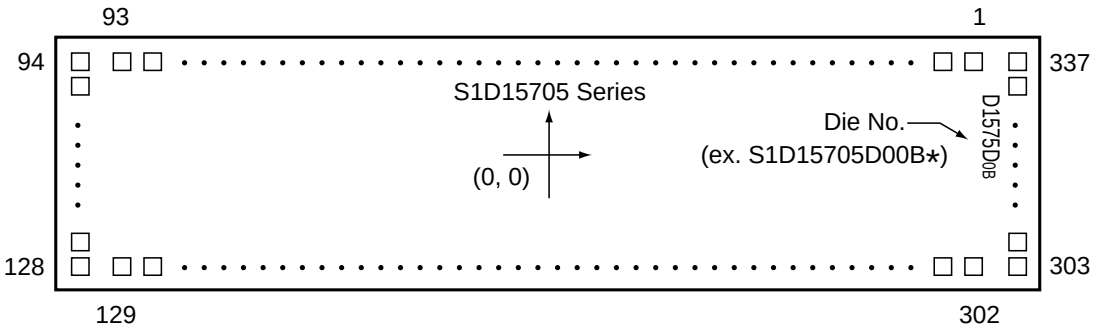
3. BLOCK DIAGRAM

Example : S1D15705*****



4. PAD

Pad layout



Item		Size X		Size Y	Unit
Chip size		13.30	×	2.81	mm
Chip thickness		0.625			mm
Bump pitch		71 (Min.)			µm
Bump size	PAD No.1 to 93	85	×	85	µm
	PAD No.94	85	×	73	µm
	PAD No.95 to 127	85	×	47	µm
	PAD No.128	85	×	73	µm
	PAD No.129	73	×	85	µm
	PAD No.130 to 301	47	×	85	µm
	PAD No.302	73	×	85	µm
	PAD No.303	86	×	73	µm
	PAD No.304 to 336	85	×	47	µm
	PAD No.337	85	×	73	µm
Bump height		17 (Typ.)			µm

S1D15705***** Pad Central Coordinates

Unit: μm

PAD No.	PIN Name	X	Y
1	(NC)	6195	1246
2	(NC)	6059	
3	SYNC	5922	
4	FRS	5786	
5	FR	5649	
6	CL	5513	
7	DOF	5376	
8	SYNC	5240	
9	VSS	5103	
10	CS1	4967	
11	CS2	4830	
12	VDD	4694	
13	RES	4557	
14	A0	4421	
15	VSS	4284	
16	WR, R/W	4148	
17	RD, E	4011	
18	VDD	3875	
19	D0	3738	
20	D1	3602	
21	D2	3465	
22	D3	3329	
23	D4	3192	
24	D5	3056	
25	D6 (SCL)	2919	
26	D7 (SI)	2783	
27	VDD	2646	
28	VDD	2512	
29	VDD	2378	
30	VDD	2245	
31	VDD	2111	
32	VSS	1977	
33	VSS	1843	
34	VSS	1709	
35	VSS2	1575	
36	VSS2	1441	
37	VSS2	1307	
38	VSS2	1173	
39	VSS2	1039	
40	(NC)	906	
41	VOUT	772	
42	VOUT	638	
43	CAP3–	504	
44	CAP3–	370	
45	(NC)	236	
46	CAP1+	102	
47	CAP1+	–32	
48	CAP1–	–166	
49	CAP1–	–300	
50	CAP2–	–433	
51	CAP2–	–567	1246
52	CAP2+	–701	
53	CAP2+	–835	
54	VSS	–969	
55	VSS	–1103	
56	VRS	–1237	
57	VRS	–1371	
58	VDD	–1505	
59	VDD	–1639	
60	V1	–1772	
61	V1	–1906	
62	V2	–2040	
63	V2	–2174	
64	(NC)	–2308	
65	V3	–2442	
66	V3	–2576	
67	V4	–2710	
68	V4	–2844	
69	V5	–2978	
70	V5	–3111	
71	(NC)	–3245	
72	VR	–3379	
73	TEST1	–3513	
74	TEST2	–3647	
75	TEST3	–3781	
76	TEST4	–3915	
77	VDD	–4049	
78	M/S	–4185	
79	CLS	–4322	
80	VSS	–4458	
81	C86	–4595	
82	P/S	–4731	
83	VDD	–4868	
84	HPM	–5004	
85	VSS	–5141	
86	IRS	–5277	
87	VDD	–5414	
88	TEST5	–5550	
89	TEST6	–5687	
90	TEST7	–5836	
91	TEST8	–5956	
92	TEST9	–6076	
93	(NC)	–6195	
94	(NC)	–6474	1248
95	COM31		1163
96	COM30		1090
97	COM29		1017
98	COM28		945
99	COM27		872
100	COM26		799
101	COM25	–6474	727
102	COM24		654
103	COM23		581
104	COM22		509
105	COM21		436
106	COM20		363
107	COM19		291
108	COM18		218
109	COM17		145
110	COM16		73
111	COM15		0
112	COM14		–73
113	COM13		–145
114	COM12		–218
115	COM11		–291
116	COM10		–363
117	COM9		–436
118	COM8		–509
119	COM7		–581
120	COM6		–654
121	COM5		–727
122	COM4		–800
123	COM3		–872
124	COM2		–945
125	COM1		–1018
126	COM0		–1090
127	COMS		–1163
128	(NC)		–1248
129	(NC)	–6232	–1246
130	(NC)	–6147	
131	(NC)	–6075	
132	SEG0	–6002	
133	SEG1	–5930	
134	SEG2	–5859	
135	SEG3	–5787	
136	SEG4	–5715	
137	SEG5	–5643	
138	SEG6	–5571	
139	SEG7	–5499	
140	SEG8	–5427	
141	SEG9	–5355	
142	SEG10	–5283	
143	SEG11	–5212	
144	SEG12	–5140	
145	SEG13	–5068	
146	SEG14	–4996	
147	SEG15	–4924	
148	SEG16	–4852	
149	SEG17	–4780	
150	SEG18	–4708	

Unit: µm

PAD No.	PIN Name	X	Y
151	SEG19	–4636	–1246
152	SEG20	–4564	
153	SEG21	–4493	
154	SEG22	–4421	
155	SEG23	–4349	
156	SEG24	–4277	
157	SEG25	–4205	
158	SEG26	–4133	
159	SEG27	–4061	
160	SEG28	–3989	
161	SEG29	–3917	
162	SEG30	–3846	
163	SEG31	–3774	
164	SEG32	–3702	
165	SEG33	–3630	
166	SEG34	–3558	
167	SEG35	–3486	
168	SEG36	–3414	
169	SEG37	–3342	
170	SEG38	–3270	
171	SEG39	–3199	
172	SEG40	–3127	
173	SEG41	–3055	
174	SEG42	–2983	
175	SEG43	–2911	
176	SEG44	–2839	
177	SEG45	–2767	
178	SEG46	–2695	
179	SEG47	–2623	
180	SEG48	–2552	
181	SEG49	–2480	
182	SEG50	–2408	
183	SEG51	–2336	
184	SEG52	–2264	
185	SEG53	–2192	
186	SEG54	–2120	
187	SEG55	–2048	
188	SEG56	–1976	
189	SEG57	–1905	
190	SEG58	–1833	
191	SEG59	–1761	
192	SEG60	–1689	
193	SEG61	–1617	
194	SEG62	–1545	
195	SEG63	–1473	
196	SEG64	–1401	
197	SEG65	–1329	
198	SEG66	–1258	
199	SEG67	–1186	
200	SEG68	–1114	

PAD No.	PIN Name	X	Y
201	SEG69	–1042	–1246
202	SEG70	–970	
203	SEG71	–898	
204	SEG72	–826	
205	SEG73	–754	
206	SEG74	–682	
207	SEG75	–611	
208	SEG76	–539	
209	SEG77	–467	
210	SEG78	–395	
211	SEG79	–323	
212	SEG80	–251	
213	SEG81	–179	
214	SEG82	–107	
215	SEG83	–35	
216	SEG84	36	
217	SEG85	108	
218	SEG86	180	
219	SEG87	252	
220	SEG88	324	
221	SEG89	396	
222	SEG90	468	
223	SEG91	540	
224	SEG92	612	
225	SEG93	683	
226	SEG94	755	
227	SEG95	827	
228	SEG96	899	
229	SEG97	971	
230	SEG98	1043	
231	SEG99	1115	
232	SEG100	1187	
233	SEG101	1259	
234	SEG102	1330	
235	SEG103	1402	
236	SEG104	1474	
237	SEG105	1546	
238	SEG106	1618	
239	SEG107	1690	
240	SEG108	1762	
241	SEG109	1834	
242	SEG110	1906	
243	SEG111	1977	
244	SEG112	2049	
245	SEG113	2121	
246	SEG114	2193	
247	SEG115	2265	
248	SEG116	2337	
249	SEG117	2409	
250	SEG118	2481	

PAD No.	PIN Name	X	Y
251	SEG119	2553	–1246
252	SEG120	2625	
253	SEG121	2696	
254	SEG122	2768	
255	SEG123	2840	
256	SEG124	2912	
257	SEG125	2984	
258	SEG126	3056	
259	SEG127	3128	
260	SEG128	3200	
261	SEG129	3272	
262	SEG130	3343	
263	SEG131	3415	
264	SEG132	3487	
265	SEG133	3559	
266	SEG134	3631	
267	SEG135	3703	
268	SEG136	3775	
269	SEG137	3847	
270	SEG138	3919	
271	SEG139	3990	
272	SEG140	4062	
273	SEG141	4134	
274	SEG142	4206	
275	SEG143	4278	
276	SEG144	4350	
277	SEG145	4422	
278	SEG146	4494	
279	SEG147	4566	
280	SEG148	4637	
281	SEG149	4709	
282	SEG150	4781	
283	SEG151	4853	
284	SEG152	4925	
285	SEG153	4997	
286	SEG154	5069	
287	SEG155	5141	
288	SEG156	5213	
289	SEG157	5284	
290	SEG158	5356	
291	SEG159	5428	
292	SEG160	5500	
293	SEG161	5572	
294	SEG162	5644	
295	SEG163	5716	
296	SEG164	5788	
297	SEG165	5860	
298	SEG166	5931	
299	SEG167	6003	
300	(NC)	6075	

Unit: μm

PAD No.	PIN Name	X	Y
301	(NC)	6147	–1246
302	(NC)	6232	↓
303	(NC)	6474	–1248
304	COM32		–1163
305	COM33		–1090
306	COM34		–1018
307	COM35		–945
308	COM36		–872
309	COM37		–800
310	COM38		–727
311	COM39		–654
312	COM40		–581
313	COM41		–509
314	COM42		–436
315	COM43		–363
316	COM44		–291
317	COM45		–218
318	COM46		–145
319	COM47		–73
320	COM48		0
321	COM49		73
322	COM50		145
323	COM51		218
324	COM52		291
325	COM53		363
326	COM54		436
327	COM55		509
328	COM56		581
329	COM57		654
330	COM58		727
331	COM59		799
332	COM60		872
333	COM61		945
334	COM62		1017
335	COM63		1090
336	COMS		1163
337	(NC)		1248

S1D15707***** Pad Central Coordinates

Unit: µm

PAD No.	PIN Name	X	Y
1	(NC)	6195	1246
2	(NC)	6059	
3	SYNC	5922	
4	FRS	5786	
5	FR	5649	
6	CL	5513	
7	DOF	5376	
8	SYNC	5240	
9	VSS	5103	
10	CS1	4967	
11	CS2	4830	
12	VDD	4694	
13	RES	4557	
14	A0	4421	
15	VSS	4284	
16	WR, R/W	4148	
17	RD, E	4011	
18	VDD	3875	
19	D0	3738	
20	D1	3602	
21	D2	3465	
22	D3	3329	
23	D4	3192	
24	D5	3056	
25	D6 (SCL)	2919	
26	D7 (SI)	2783	
27	VDD	2646	
28	VDD	2512	
29	VDD	2378	
30	VDD	2245	
31	VDD	2111	
32	VSS	1977	
33	VSS	1843	
34	VSS	1709	
35	VSS2	1575	
36	VSS2	1441	
37	VSS2	1307	
38	VSS2	1173	
39	VSS2	1039	
40	(NC)	906	
41	VOUT	772	
42	VOUT	638	
43	CAP3–	504	
44	CAP3–	370	
45	(NC)	236	
46	CAP1+	102	
47	CAP1+	–32	
48	CAP1–	–166	
49	CAP1–	–300	
50	CAP2–	–433	
51	CAP2–	–567	1246
52	CAP2+	–701	
53	CAP2+	–835	
54	VSS	–969	
55	VSS	–1103	
56	VRS	–1237	
57	VRS	–1371	
58	VDD	–1505	
59	VDD	–1639	
60	V1	–1772	
61	V1	–1906	
62	V2	–2040	
63	V2	–2174	
64	(NC)	–2308	
65	V3	–2442	
66	V3	–2576	
67	V4	–2710	
68	V4	–2844	
69	V5	–2978	
70	V5	–3111	
71	(NC)	–3245	
72	VR	–3379	
73	TEST1	–3513	
74	TEST2	–3647	
75	TEST3	–3781	
76	TEST4	–3915	
77	VDD	–4049	
78	M/S	–4185	
79	CLS	–4322	
80	VSS	–4458	
81	C86	–4595	
82	P/S	–4731	
83	VDD	–4868	
84	HPM	–5004	
85	VSS	–5141	
86	IRS	–5277	
87	VDD	–5414	
88	TEST5	–5550	
89	TEST6	–5687	
90	TEST7	–5836	
91	TEST8	–5956	
92	TEST9	–6076	
93	(NC)	–6195	
94	(NC)	–6474	1248
95	COM31		1163
96	COM30		1090
97	COM29		1017
98	COM28		945
99	COM27		872
100	COM26		799
101	COM25	–6474	727
102	COM24		654
103	COM23		581
104	COM22		509
105	COM21		436
106	COM20		363
107	COM19		291
108	COM18		218
109	COM17		145
110	COM16		73
111	COM15		0
112	COM14		–73
113	COM13		–145
114	COM12		–218
115	COM11		–291
116	COM10		–363
117	COM9		–436
118	COM8		–509
119	COM7		–581
120	COM6		–654
121	COM5		–727
122	COM4		–800
123	COM3		–872
124	COM2		–945
125	COM1		–1018
126	COM0		–1090
127	COMS		–1163
128	(NC)		–1248
129	(NC)	–6232	–1246
130	(NC)	–6147	
131	(NC)	–6075	
132	SEG0	–6002	
133	SEG1	–5930	
134	SEG2	–5859	
135	SEG3	–5787	
136	SEG4	–5715	
137	SEG5	–5643	
138	SEG6	–5571	
139	SEG7	–5499	
140	SEG8	–5427	
141	SEG9	–5355	
142	SEG10	–5283	
143	SEG11	–5212	
144	SEG12	–5140	
145	SEG13	–5068	
146	SEG14	–4996	
147	SEG15	–4924	
148	SEG16	–4852	
149	SEG17	–4780	
150	SEG18	–4708	

Unit: μm

PAD No.	PIN Name	X	Y
151	SEG19	–4636	–1246
152	SEG20	–4564	
153	SEG21	–4493	
154	SEG22	–4421	
155	SEG23	–4349	
156	SEG24	–4277	
157	SEG25	–4205	
158	SEG26	–4133	
159	SEG27	–4061	
160	SEG28	–3989	
161	SEG29	–3917	
162	SEG30	–3846	
163	SEG31	–3774	
164	SEG32	–3702	
165	SEG33	–3630	
166	SEG34	–3558	
167	SEG35	–3486	
168	SEG36	–3414	
169	SEG37	–3342	
170	SEG38	–3270	
171	SEG39	–3199	
172	SEG40	–3127	
173	SEG41	–3055	
174	SEG42	–2983	
175	SEG43	–2911	
176	SEG44	–2839	
177	SEG45	–2767	
178	SEG46	–2695	
179	SEG47	–2623	
180	SEG48	–2552	
181	SEG49	–2480	
182	SEG50	–2408	
183	SEG51	–2336	
184	SEG52	–2264	
185	SEG53	–2192	
186	SEG54	–2120	
187	SEG55	–2048	
188	SEG56	–1976	
189	SEG57	–1905	
190	SEG58	–1833	
191	SEG59	–1761	
192	SEG60	–1689	
193	SEG61	–1617	
194	SEG62	–1545	
195	SEG63	–1473	
196	SEG64	–1401	
197	SEG65	–1329	
198	SEG66	–1258	
199	SEG67	–1186	
200	SEG68	–1114	

PAD No.	PIN Name	X	Y
201	SEG69	–1042	–1246
202	SEG70	–970	
203	SEG71	–898	
204	SEG72	–826	
205	SEG73	–754	
206	SEG74	–682	
207	SEG75	–611	
208	SEG76	–539	
209	SEG77	–467	
210	SEG78	–395	
211	SEG79	–323	
212	SEG80	–251	
213	SEG81	–179	
214	SEG82	–107	
215	SEG83	–35	
216	SEG84	36	
217	SEG85	108	
218	SEG86	180	
219	SEG87	252	
220	SEG88	324	
221	SEG89	396	
222	SEG90	468	
223	SEG91	540	
224	SEG92	612	
225	SEG93	683	
226	SEG94	755	
227	SEG95	827	
228	SEG96	899	
229	SEG97	971	
230	SEG98	1043	
231	SEG99	1115	
232	SEG100	1187	
233	SEG101	1259	
234	SEG102	1330	
235	SEG103	1402	
236	SEG104	1474	
237	SEG105	1546	
238	SEG106	1618	
239	SEG107	1690	
240	SEG108	1762	
241	SEG109	1834	
242	SEG110	1906	
243	SEG111	1977	
244	SEG112	2049	
245	SEG113	2121	
246	SEG114	2193	
247	SEG115	2265	
248	SEG116	2337	
249	SEG117	2409	
250	SEG118	2481	

PAD No.	PIN Name	X	Y
251	SEG119	2553	–1246
252	SEG120	2625	
253	SEG121	2696	
254	SEG122	2768	
255	SEG123	2840	
256	SEG124	2912	
257	SEG125	2984	
258	SEG126	3056	
259	SEG127	3128	
260	SEG128	3200	
261	SEG129	3272	
262	SEG130	3343	
263	SEG131	3415	
264	SEG132	3487	
265	SEG133	3559	
266	SEG134	3631	
267	SEG135	3703	
268	SEG136	3775	
269	SEG137	3847	
270	SEG138	3919	
271	SEG139	3990	
272	SEG140	4062	
273	SEG141	4134	
274	SEG142	4206	
275	SEG143	4278	
276	SEG144	4350	
277	SEG145	4422	
278	SEG146	4494	
279	SEG147	4566	
280	SEG148	4637	
281	SEG149	4709	
282	SEG150	4781	
283	SEG151	4853	
284	SEG152	4925	
285	SEG153	4997	
286	SEG154	5069	
287	SEG155	5141	
288	SEG156	5213	
289	SEG157	5284	
290	SEG158	5356	
291	SEG159	5428	
292	SEG160	5500	
293	SEG161	5572	
294	SEG162	5644	
295	SEG163	5716	
296	SEG164	5788	
297	SEG165	5860	
298	SEG166	5931	
299	SEG167	6003	
300	(NC)	6075	

Unit: μm

PAD No.	PIN Name	X	Y
301	(NC)	6147	–1246
302	(NC)	6232	↓
303	(NC)	6474	–1248
304	SEG168		–1163
305	SEG169		–1090
306	SEG170		–1018
307	SEG171		–945
308	SEG172		–872
309	SEG173		–800
310	SEG174		–727
311	SEG175		–654
312	SEG176		–581
313	SEG177		–509
314	SEG178		–436
315	SEG179		–363
316	SEG180		–291
317	SEG181		–218
318	SEG182		–145
319	SEG183		–73
320	SEG184		0
321	SEG185		73
322	SEG186		145
323	SEG187		218
324	SEG188		291
325	SEG189		363
326	SEG190		436
327	SEG191		509
328	SEG192		581
329	SEG193		654
330	SEG194		727
331	SEG195		799
332	SEG196		872
333	SEG197		945
334	SEG198		1017
335	SEG199		1090
336	COMS		1163
337	(NC)		1248

S1D15708***** Pad Central Coordinates

Unit: µm

PAD No.	PIN Name	X	Y
1	(NC)	6159	1246
2	(NC)	6059	
3	SYNC	5922	
4	FRS	5786	
5	FR	5649	
6	CL	5513	
7	DOF	5376	
8	SYNC	5240	
9	VSS	5103	
10	CS1	4967	
11	CS2	4830	
12	VDD	4694	
13	RES	4557	
14	A0	4421	
15	VSS	4284	
16	WR,R/W	4148	
17	RD, E	4011	
18	VDD	3875	
19	D0	3738	
20	D1	3602	
21	D2	3465	
22	D3	3329	
23	D4	3192	
24	D5	3056	
25	D6 (SCL)	2919	
26	D7 (SI)	2783	
27	VDD	2646	
28	VDD	2512	
29	VDD	2378	
30	VDD	2245	
31	VDD	2111	
32	VSS	1977	
33	VSS	1843	
34	VSS	1709	
35	VSS2	1575	
36	VSS2	1441	
37	VSS2	1307	
38	VSS2	1173	
39	VSS2	1039	
40	(NC)	906	
41	VOUT	772	
42	VOUT	638	
43	CAP3–	504	
44	CAP3–	370	
45	(NC)	236	
46	CAP1+	102	
47	CAP1+	–32	
48	CAP1–	–166	
49	CAP1–	–300	
50	CAP2–	–433	
51	CAP2–	–567	1246
52	CAP2+	–701	
53	CAP2+	–835	
54	VSS	–969	
55	VSS	–1103	
56	VRS	–1237	
57	VRS	–1371	
58	VDD	–1505	
59	VDD	–1639	
60	V1	–1772	
61	V1	–1906	
62	V2	–2040	
63	V2	–2174	
64	(NC)	–2308	
65	V3	–2442	
66	V3	–2576	
67	V4	–2710	
68	V4	–2844	
69	V5	–2978	
70	V5	–3111	
71	(NC)	–3245	
72	VR	–3379	
73	TEST1	–3513	
74	TEST2	–3647	
75	TEST3	–3781	
76	TEST4	–3915	
77	VDD	–4049	
78	M/S	–4185	
79	CLS	–4322	
80	VSS	–4458	
81	C86	–4595	
82	P/S	–4731	
83	VDD	–4868	
84	HPM	–5004	
85	VSS	–5141	
86	IRS	–5277	
87	VDD	–5414	
88	TEST5	–5550	
89	TEST6	–5687	
90	TEST7	–5836	
91	TEST8	–5956	
92	TEST9	–6076	
93	(NC)	–6195	
94	(NC)	–6474	1248
95	COM15		1163
96	COM15		1090
97	COM14		1017
98	COM14		945
99	COM13		872
100	COM13		799
101	COM12	–6474	727
102	COM12		654
103	COM11		581
104	COM11		509
105	COM10		436
106	COM10		363
107	COM9		291
108	COM9		218
109	COM8		145
110	COM8		73
111	COM7		0
112	COM7		–73
113	COM6		–145
114	COM6		–218
115	COM5		–291
116	COM5		–363
117	COM4		–436
118	COM4		–509
119	COM3		–581
120	COM3		–654
121	COM2		–727
122	COM2		–800
123	COM1		–872
124	COM1		–945
125	COM0		–1018
126	COM0		–1090
127	COMS		–1163
128	(NC)		–1248
129	(NC)	–6232	–1246
130	(NC)	–6147	
131	(NC)	–6075	
132	SEG0	–6002	
133	SEG1	–5930	
134	SEG2	–5859	
135	SEG3	–5787	
136	SEG4	–5715	
137	SEG5	–5643	
138	SEG6	–5571	
139	SEG7	–5499	
140	SEG8	–5427	
141	SEG9	–5355	
142	SEG10	–5283	
143	SEG11	–5212	
144	SEG12	–5140	
145	SEG13	–5068	
146	SEG14	–4996	
147	SEG15	–4924	
148	SEG16	–4852	
149	SEG17	–4780	
150	SEG18	–4708	

Unit: µm

PAD No.	PIN Name	X	Y
151	SEG19	–4636	–1246
152	SEG20	–4564	
153	SEG21	–4493	
154	SEG22	–4421	
155	SEG23	–4349	
156	SEG24	–4277	
157	SEG25	–4205	
158	SEG26	–4133	
159	SEG27	–4061	
160	SEG28	–3989	
161	SEG29	–3917	
162	SEG30	–3846	
163	SEG31	–3774	
164	SEG32	–3702	
165	SEG33	–3630	
166	SEG34	–3558	
167	SEG35	–3486	
168	SEG36	–3414	
169	SEG37	–3342	
170	SEG38	–3270	
171	SEG39	–3199	
172	SEG40	–3127	
173	SEG41	–3055	
174	SEG42	–2983	
175	SEG43	–2911	
176	SEG44	–2839	
177	SEG45	–2767	
178	SEG46	–2695	
179	SEG47	–2623	
180	SEG48	–2552	
181	SEG49	–2480	
182	SEG50	–2408	
183	SEG51	–2336	
184	SEG52	–2264	
185	SEG53	–2192	
186	SEG54	–2120	
187	SEG55	–2048	
188	SEG56	–1976	
189	SEG57	–1905	
190	SEG58	–1833	
191	SEG59	–1761	
192	SEG60	–1689	
193	SEG61	–1617	
194	SEG62	–1545	
195	SEG63	–1473	
196	SEG64	–1401	
197	SEG65	–1329	
198	SEG66	–1258	
199	SEG67	–1186	
200	SEG68	–1114	

PAD No.	PIN Name	X	Y
201	SEG69	–1042	–1246
202	SEG70	–970	
203	SEG71	–898	
204	SEG72	–826	
205	SEG73	–754	
206	SEG74	–682	
207	SEG75	–611	
208	SEG76	–539	
209	SEG77	–467	
210	SEG78	–395	
211	SEG79	–323	
212	SEG80	–251	
213	SEG81	–179	
214	SEG82	–107	
215	SEG83	–35	
216	SEG84	36	
217	SEG85	108	
218	SEG86	180	
219	SEG87	252	
220	SEG88	324	
221	SEG89	396	
222	SEG90	468	
223	SEG91	540	
224	SEG92	612	
225	SEG93	683	
226	SEG94	755	
227	SEG95	827	
228	SEG96	899	
229	SEG97	971	
230	SEG98	1043	
231	SEG99	1115	
232	SEG100	1187	
233	SEG101	1259	
234	SEG102	1330	
235	SEG103	1402	
236	SEG104	1474	
237	SEG105	1546	
238	SEG106	1618	
239	SEG107	1690	
240	SEG108	1762	
241	SEG109	1834	
242	SEG110	1906	
243	SEG111	1977	
244	SEG112	2049	
245	SEG113	2121	
246	SEG114	2193	
247	SEG115	2265	
248	SEG116	2337	
249	SEG117	2409	
250	SEG118	2481	

PAD No.	PIN Name	X	Y
251	SEG119	2553	–1246
252	SEG120	2625	
253	SEG121	2696	
254	SEG122	2768	
255	SEG123	2840	
256	SEG124	2912	
257	SEG125	2984	
258	SEG126	3056	
259	SEG127	3128	
260	SEG128	3200	
261	SEG129	3272	
262	SEG130	3343	
263	SEG131	3415	
264	SEG132	3487	
265	SEG133	3559	
266	SEG134	3631	
267	SEG135	3703	
268	SEG136	3775	
269	SEG137	3847	
270	SEG138	3919	
271	SEG139	3990	
272	SEG140	4062	
273	SEG141	4134	
274	SEG142	4206	
275	SEG143	4278	
276	SEG144	4350	
277	SEG145	4422	
278	SEG146	4494	
279	SEG147	4566	
280	SEG148	4637	
281	SEG149	4709	
282	SEG150	4781	
283	SEG151	4853	
284	SEG152	4925	
285	SEG153	4997	
286	SEG154	5069	
287	SEG155	5141	
288	SEG156	5213	
289	SEG157	5284	
290	SEG158	5356	
291	SEG159	5428	
292	SEG160	5500	
293	SEG161	5572	
294	SEG162	5644	
295	SEG163	5716	
296	SEG164	5788	
297	SEG165	5860	
298	SEG166	5931	
299	SEG167	6003	
300	(NC)	6075	

Unit: μm

PAD No.	PIN Name	X	Y
301	(NC)	6147	–1246
302	(NC)	6232	↓
303	(NC)	6474	–1248
304	SEG168		–1163
305	SEG169		–1090
306	SEG170		–1018
307	SEG171		–945
308	SEG172		–872
309	SEG173		–800
310	SEG174		–727
311	SEG175		–654
312	SEG176		–581
313	SEG177		–509
314	SEG178		–436
315	SEG179		–363
316	SEG180		–291
317	SEG181		–218
318	SEG182		–145
319	SEG183		–73
320	SEG184		0
321	SEG185		73
322	SEG186		145
323	SEG187		218
324	SEG188		291
325	SEG189		363
326	SEG190		436
327	SEG191		509
328	SEG192		581
329	SEG193		654
330	SEG194		727
331	SEG195		799
332	SEG196		872
333	SEG197		945
334	SEG198		1017
335	SEG199		1090
336	COMS		1163
337	(NC)		1248

5. PIN DESCRIPTION

Power Supply Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>V_{DD}</td><td>Power supply</td><td>Commonly used with the MPU power supply pin V_{CC}.</td><td>12</td></tr>
<tr><td>V_{SS}</td><td>Power supply</td><td>0 V pin connected to the system ground (GND).</td><td>9</td></tr>
<tr><td>V_{SS2}</td><td>Power supply</td><td>Boosting circuit reference power supply for liquid crystal drive.</td><td>5</td></tr>
<tr><td>V_{RS}</td><td>Power supply</td><td>External input pin for liquid crystal power supply voltage adjusting circuit.
They are set to OPEN.</td><td>2</td></tr>
<tr><td>V_1, V_2
V_3, V_4
V_5</td><td>Power supply</td><td>Multi-level power supply for liquid crystal drive. The voltage specified according to liquid crystal cells is impedance-converted by a split resistor or operation amplifier (OP amp) and applied. The potential needs to be specified based on V_{DD} to establish the relationship of dimensions shown below:
V_{DD} (=V_0) ≥ V_1 ≥ V_2 ≥ V_3 ≥ V_4 ≥ V_5
Master operation When the power supply is ON, the following voltages are applied to V_1 to V_4 from the built-in power supply circuit. The selection of the voltages is determined using the LCD bias set command.
<table>
<tr><td></td><td colspan="2">S1D15705***</td><td colspan="2">S1D15707***, S1D15708***</td></tr>
<tr><td>V_1</td><td>1/9•V_5</td><td>1/7•V_5</td><td>1/6•V_5</td><td>1/5•V_5</td></tr>
<tr><td>V_2</td><td>2/9•V_5</td><td>2/7•V_5</td><td>2/6•V_5</td><td>2/5•V_5</td></tr>
<tr><td>V_3</td><td>7/9•V_5</td><td>5/7•V_5</td><td>4/6•V_5</td><td>3/5•V_5</td></tr>
<tr><td>V_4</td><td>8/9•V_5</td><td>6/7•V_5</td><td>5/6•V_5</td><td>4/5•V_5</td></tr>
</table></td><td>10</td></tr>
</table>

LCD Power Supply Circuit Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CAP1+</td><td>O</td><td>Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP1– pin.</td><td>2</td></tr>
<tr><td>CAP1–</td><td>O</td><td>Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.</td><td>2</td></tr>
<tr><td>CAP2+</td><td>O</td><td>Boosting capacitor positive side connecting pin. Connects a capacitor between the pin and CAP2– pin.</td><td>2</td></tr>
<tr><td>CAP2–</td><td>O</td><td>Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP2+ pin.</td><td>2</td></tr>
<tr><td>CAP3–</td><td>O</td><td>Boosting capacitor negative side connecting pin. Connects a capacitor between the pin and CAP1+ pin.</td><td>2</td></tr>
<tr><td>V_{OUT}</td><td>O</td><td>Boosting output pin. Connects a capacitor between the pin and V_{SS2}.</td><td>2</td></tr>
<tr><td>V_R</td><td>I</td><td>Voltage adjusting pin. Applies voltage between V_{DD} and V_5 using a split resistor.
Valid only when the V_5 voltage adjusting built-in resistor is not used (IRS=LOW)
Do not use VR when the V_5 voltage adjusting built-in resistor is used (IRS=HIGH)</td><td>1</td></tr>
</table>

System Bus Connecting Pins

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0
(SI)
(SCL)</td><td>I/O</td><td>An 8-bit bidirectional data bus is used to connect an 8-bit or 16-bit standard MPU data bus.
When the serial interface is selected (P/S=LOW),
D7: Serial data entry pin (SI)
D6: Serial clock input pin (SCL)
In this case, D0 to D5 are set to high impedance.
When Chip Select is in the non-active state, D0 to D7 are set to high impedance.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Normally the lowest order bit of the MPU address bus is connected to discriminate data / commands.
A0=HIGH: Indicates that D0 to D7 are display data.
A0=LOW: Indicates that D0 to D7 are control data.</td><td>1</td></tr>
<tr><td>RES</td><td>I</td><td>Initialized by setting $\overline{RES}$ to LOW.
Reset operation is performed at the $\overline{RES}$ signal level.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>Chip Select signal. When $\overline{CS1}$=LOW and CS2=HIGH, this signal becomes active and the input/output of data/commands is enabled.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{RD}$ signal of the 80 series MPU. When this signal is LOW, the S1D15705 series data bus is set in the output state.
• When the 68 series MPU is connected, active HIGH is set.
68 series MPU enable clock input pin</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected, active LOW is set.
Pin that connects the $\overline{WR}$ signal of the 80 series MPU. The data bus signal is latched on the leading edge of the $\overline{WR}$ signal.
• When the 68 series MPU is connected,
Read/write control signal input pin
R/$\overline{W}$=HIGH: Read operation
R/$\overline{W}$=LOW: Write operation</td><td>1</td></tr>
<tr><td>FRS</td><td>O</td><td>Output pin for static drive
Used together with the SYNC pin</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>MPU interface switching pin
C86=HIGH: 68 series MPU interface
C86=LOW: 80 series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Switching pin for parallel data entry/serial data entry
P/S=HIGH: Parallel data entry
P/S=LOW: Serial data entry
According to the P/S state, the following table is given.
<table>
<tr><th>P/S</th><th>Data/ command</th><th>Data</th><th>Read/write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write-only</td><td>SCL (D6)</td></tr>
</table>
When P/S=LOW, D0 to D5 are set to high impedance. D0 to D5 can be HIGH, LOW, or “OPEN”.
RD(E) and WR (R/W) are fixed to HIGH or LOW.
For the serial data entry, RAM display data cannot be read.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>Pin that selects the validity/invalidity of the built-in oscillator circuit for display clocks.
CLS=HIGH: Built-in oscillator circuit valid
CLS=LOW: Built-in oscillator circuit invalid (external input)
When CLS=LOW, display clocks are input from the CL pin.
When the S1D15705 series is used for the master/slave configuration, each of the CLS pins is set to the same level together.
<table>
<tr><th>Display clock</th><th>Master</th><th>Slave</th></tr>
<tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr>
<tr><td>External input</td><td>LOW</td><td>LOW</td></tr>
</table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>Pin that selects the master/slave operation for the S1D15705 series. The liquid crystal display system is synchronized by outputting the timing signal required for the liquid crystal display for the master operation and inputting the timing signal required for the liquid crystal display for the slave operation.
M/S=HIGH : Master operation
M/S=LOW : Slave operation
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>Oscillator circuit</th><th>Power supply circuit</th><th>CL</th><th>FR</th><th>SYNC</th><th>FRS</th><th>DOF</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>Valid</td><td>Valid</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td></td><td>LOW</td><td>Invalid</td><td>Valid</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
<tr><td></td><td>LOW</td><td>Invalid</td><td>Invalid</td><td>Input</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock I/O pin
According to the M/S and CLS states, the following table is given.
<table>
<tr><th>M/S</th><th>CLS</th><th>CL</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>Output</td></tr>
<tr><td></td><td>LOW</td><td>Input</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>Input</td></tr>
<tr><td></td><td>LOW</td><td>Input</td></tr>
</table>
When the S1D15705 series is used for the master/slave configuration, each CL pin is connected.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>Liquid crystal alternating current signal I/O pin
M/S=HIGH : Output
M/S=LOW : Input
When the S1D15705 series is used for the master/slave configuration, each FR pin is connected.</td><td>1</td></tr>
<tr><td>SYNC</td><td>I/O</td><td>Liquid crystal synchronizing current signal I/O pin
M/S=HIGH : Output
M/S=LOW : Input
When the S1D15705 series is used for the master/slave configuration, each SYNC pin is connected.</td><td>2</td></tr>
<tr><td>$\overline{DOF}$</td><td>I/O</td><td>Liquid crystal display blanking control pin
M/S=HIGH : Output
M/S=LOW : Input
When the S1D15705 series is used for the master/slave configuration, each $\overline{DOF}$ pin is connected.</td><td>1</td></tr>
<tr><td>IRS</td><td>I</td><td>V_5 voltage adjusting resistor selection pin
IRS=HIGH: Built-in resistor used
IRS=LOW: Built-in resistor not used. The V_5 voltage is adjusted by the VR pin and stand-alone split resistor.
Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.</td><td>1</td></tr>
<tr><td>$\overline{HPM}$</td><td>I</td><td>Power supply control pin of the power supply circuit for liquid crystal drive
$\overline{HPM}$=HIGH : Normal mode
$\overline{HPM}$=LOW : High power supply mode
Valid only at master operation. The pin is fixed to HIGH or LOW at slave operation.</td><td>1</td></tr>
</table>

Liquid Crystal Drive Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>SEG0
to
SEGn</td><td>O</td><td>Output pins for the LCD segment drive.
For the pin assignment by model, refer to the table below.
<table>
<tr><th>Product name</th><th>SEG</th><th>Number of pins</th></tr>
<tr><td>S1D15705*****</td><td>SEG0 to SEG167</td><td>168</td></tr>
<tr><td>S1D15707*****/S1D15708*****</td><td>SEG0 to SEG199</td><td>200</td></tr>
</table>
Contents of the display RAM and FR signal are combined to select a desired level among V_{DD}, V_2, V_3 and V_5.
<table>
<tr><th rowspan="2">RAM data</th><th rowspan="2">FR</th><th colspan="2">Output voltage</th></tr>
<tr><th>Display normal operation</th><th>Display reversal</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_{DD}</td><td>V_2</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_5</td><td>V_3</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_2</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_3</td><td>V_5</td></tr>
<tr><td>Power save</td><td>—</td><td colspan="2">V_{DD}</td></tr>
</table></td><td>168 or 200</td></tr>
<tr><td>COM0
to
COMn</td><td></td><td>Output pins for the LCD common drive.
For the pin assignment by model, refer to the table below.
<table>
<tr><th>Product name</th><th>SEG</th><th>Number of pins</th></tr>
<tr><td>S1D15705*****</td><td>COM0 to COM63</td><td>64</td></tr>
<tr><td>S1D15707*****</td><td>COM0 to COM31</td><td>32</td></tr>
<tr><td>S1D15708*****</td><td>COM0 to COM15</td><td>16</td></tr>
</table>
Scan data and FR signal are combined to select a desired level among V_{DD}, V_1, V_4 and V_5.
<table>
<tr><th>Scanning data</th><th>FR</th><th>Output voltage</th></tr>
<tr><td>HIGH</td><td>HIGH</td><td>V_5</td></tr>
<tr><td>HIGH</td><td>LOW</td><td>V_{DD}</td></tr>
<tr><td>LOW</td><td>HIGH</td><td>V_1</td></tr>
<tr><td>LOW</td><td>LOW</td><td>V_4</td></tr>
<tr><td>Power save</td><td>—</td><td>V_{DD}</td></tr>
</table></td><td>64 or 32
or 16</td></tr>
<tr><td>COMS</td><td>O</td><td>Indicator dedicated COM output pin. Set to OPEN when not used.
When COMS is used for the master/slave configuration, the same signal is output to both the master and slave.</td><td>2</td></tr>
</table>

Test Pin

Pin name	I/O	Description	Number of pins
TEST1 to 6	I/O	IC chip test pin. Fix the pin to HIGH. When using the temperature sensor with the S1D15705⋆10⋆⋆, refer to “Section 17. Temperature Sensor Circuit”.	6
TEST7 to 9	I/O	IC chip test pin. Take into consideration so that the capacity of lines cannot be exhausted by setting the pin to OPEN.	3

6. FUNCTION DESCRIPTION

MPU Interface

Selection of interface type

The S1D15705 series transfers data through 8-bit bidirectional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to either HIGH or LOW, the 8-bit parallel data entry or serial data entry can be selected as listed in Table 1.

Table 1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH: Parallel data entry	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW: Serial data entry	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

Fix — to HIGH or LOW. HZ indicates the high impedance state.

Parallel interface

When the parallel interface is selected (P/S=HIGH), the S1D15705 series can directly be connected to the MPU bus of either the 80 or 68 series MPU by setting the C86 pin to HIGH or LOW as listed in Table 2.

Table 2

C86	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
H: 68 series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
L: 80 series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

In addition, the data bus signal can be identified according to the combinations of the A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$) signals as listed in Table 3.

Table 3

Common	68 series	80 series		
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	Function
1	1	0	1	Display data read
1	0	1	0	Display data write
0	1	0	1	Status read
0	0	1	0	Control data write (command)

Serial interface

When the serial interface is selected (P/S=LOW), the serial data entry (SI) and serial clock input(SCL) can be accepted with the chip in the non-active state ($\overline{CS1}$=LOW or CS2=HIGH. The serial interface consists of an 8-bit shift register and a 3-bit counter. Serial data is fetched from the serial data entry pin in the order of D7, D6, ..., and D0 on the leading edge of the serial clock and converted into 8-bit parallel data on the leading edge of the 8th serial clock, then processed.
Whether to identify that the serial data entry is display data or command is judged by the A0 input, and A0=HIGH indicates display data and A0=LOW indicates the command. After the chip is set to the non-active state, the A0 input is read and identified at the timing on the $8 \times$ n-th leading edge of the serial clock. Fig. 1 shows the signal chart of the serial interface.

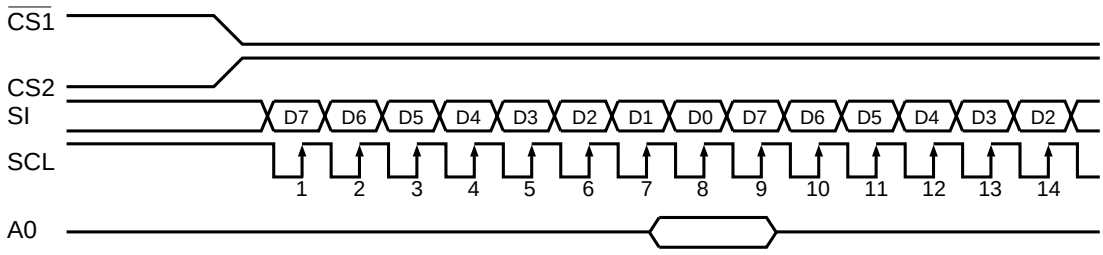


Fig. 1

- When the chip is in the non-active state, both the shift register and counter are reset to the initial state.
- Cannot be read for the serial interface.
- For the SCL signal, pay careful attention to the terminating reflection of lines and external noise. The operation confirmation using actual equipment is recommended.

Chip select

The S1D15705 series has two chip select pins $\overline{CS1}$ and CS2 and enables the MPU interface or serial interface only when $\overline{CS1}$=LOW and CS2=HIGH.
When Chip Select is in the non-active state, D0 to D7 are in the high impedance state and the A0, $\overline{RD}$, and $\overline{WR}$ inputs become invalid. When the serial interface is selected, the shift register and counter are reset.

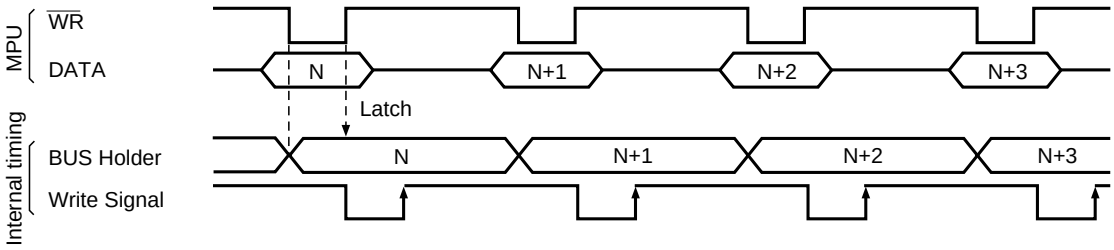
Display data RAM and internal register access

Since the S1D15705 series access viewed from the MUP side satisfies the cycle time and does not require the wait time, high-speed data transfer is enabled.
The S1D15705 series performs a kind of inter-LSI pipeline processing through the bus holder attached to the internal data bus when it performs the data transfer with the MPU.
For example, when data is written on the display data RAM, the data is first held in the bus holder and written on the display data RAM up to the next data write cycle. Further, when the MPU reads the contents of display data RAM, the read data at the first data read cycle (dummy) is held in the bus holder and read on the system bus from the bus holder up to the next data read cycle. The read sequence of the display data RAM is restricted. When the address is set, note that the specified address data is not output to the subsequent read instruction and output at the second data read. Therefore single dummy read is required after the address set and write cycle. Fig. 2 shows this relationship.

Busy flag

When the busy flag is “1”, it indicates that the S1D15705 series is performing an internal operation, and only the status read instruction can be accepted. The busy flag is output to the D7 pin using the status read command. If the cycle time (t_{CYC}) is ensured, the MPU throughput can be improved greatly since this flag needs not be checked before each command.

• Write



• Read

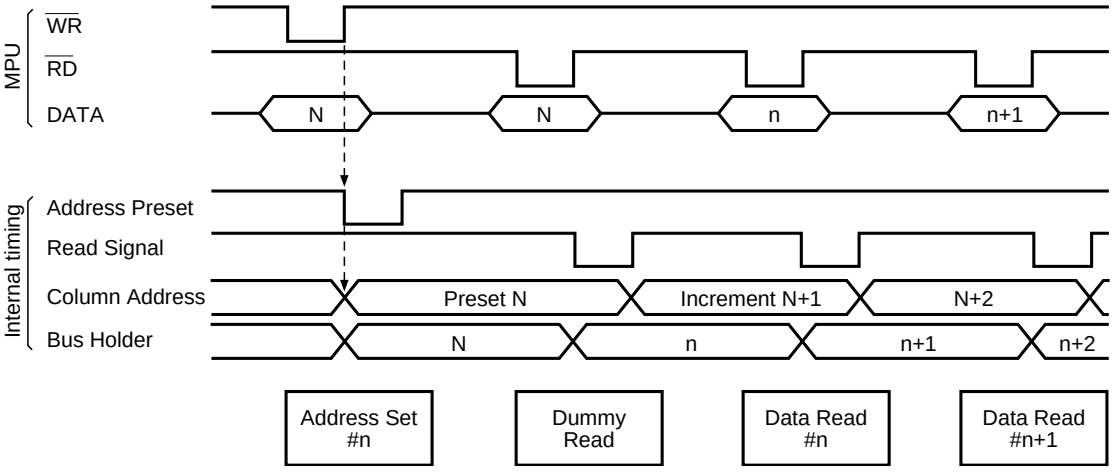


Fig. 2

Display Data RAM

Display data RAM

This display data RAM stores display dot data and consists of 65 (8 pages × one 8 bit + 1) × 200 bits. Desired bits can be accessed by specifying page and column addresses.
Since the MPU display data D7 to D0 correspond to the common direction of the liquid crystal display, the restrictions at display data transfer is reduced and the display configuration with the high degree of freedom can easily be obtained when the S1D15705 series is used for the multiple chip configuration.
Besides, the read/write operation to the display data RAM is performed through the I/O buffer from the MPU side independently of the liquid crystal drive signal read. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.

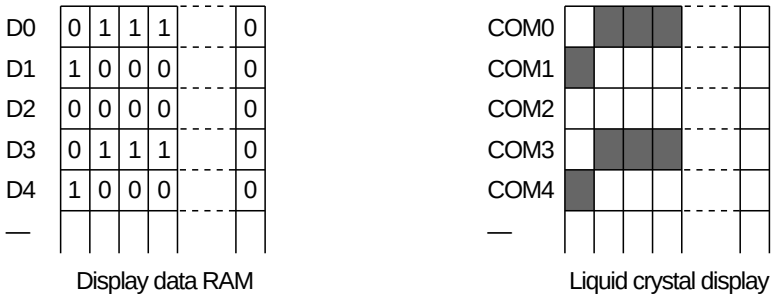


Fig. 3

Page address circuit

As shown in Fig. 4, the page address of the display data RAM is specified using the page address set command. To access the data using a new page, the page address is respecified.
The page address 8 (D3,D2,D1,D0=1,0,0,0) is an indicator dedicated RAM area and only the display data D0 is valid.

Column address circuit

As shown in Fig. 4, an address on the column side of the display data RAM is specified using the column address set command. Since the specified address is incremented by 1 whenever the display data read/write command is input, the MPU can successively access the display data.
Besides, the column address stops the increment at the column C7H. Since the column and page addresses are independent each other, for example, the page and column addresses need to be respecified respectively to move from the column C7H of page 0 and column 00H.
Further, as shown in Fig. 4, the correspondence relationship between the column address of the display data RAM and the segment address can be reversed using the ADC command (segment driver direction select command). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 4

	S1D15705***	**S1D15707***** / S1D15708*****
SEG output	SEG0 SEG167	SEG0 SEG199
ADC "0"	0 (H)→ Column Address→ A7 (H)	0 (H)→ Column Address→ C7 (H)
(D0) "1"	C7 (H)←Column Address← 20 (H)	C7 (H)←Column Address ← 0 (H)

Line address circuit

When displaying contents of the display data RAM, the line address circuit is used for specifying the corresponding addresses. See Figure 4-1 and 4-2. Using the display start line address set command, the top line is normally selected (when the common output state is normal, COM0 is output. And, when reversed, the S1D15705***** outputs COM63, S1D15707***** outputs COM31 and S1D15708*****outputs COM15). For the S1D15705*****, the display area of 65 lines is secured starting from the specified display start line address in the address incrementing direction. And, 33 lines are provided for the S1D15707*****, 17 lines are provided for the S1D15708*****.
Dynamically changing the line address using the display start line address set command enables screen scrolling and page change.

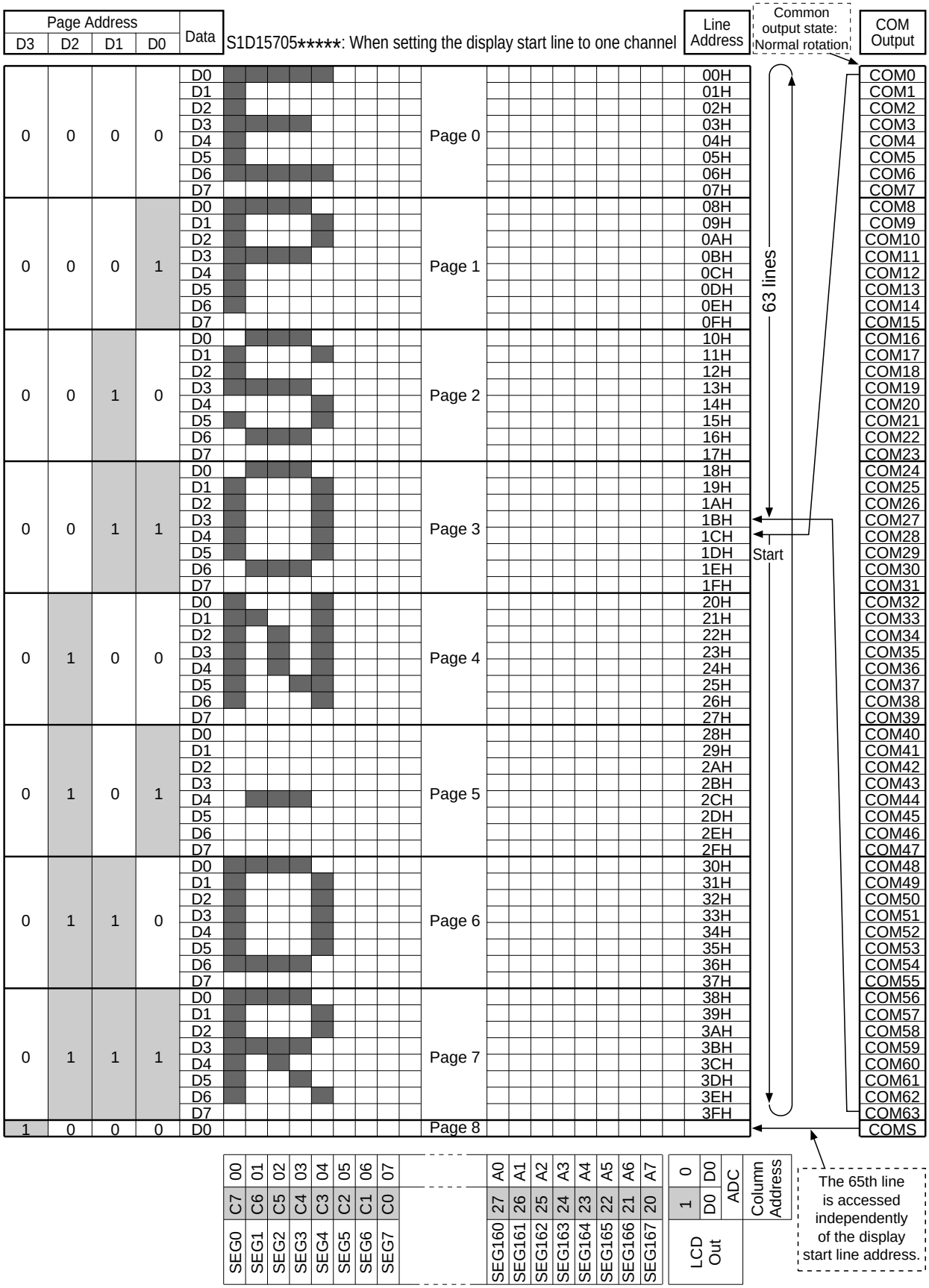

Page Address
D3 D2 D1 D0
Data
S1D15705*****: When setting the display start line to one channel
Line Address
Common output state: Normal rotation
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
63 lines
Start
The 65th line is accessed independently of the display start line address.
Column Address
ADC
LCD Out
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG160 SEG161 SEG162 SEG163 SEG164 SEG165 SEG166 SEG167

Fig. 4-1

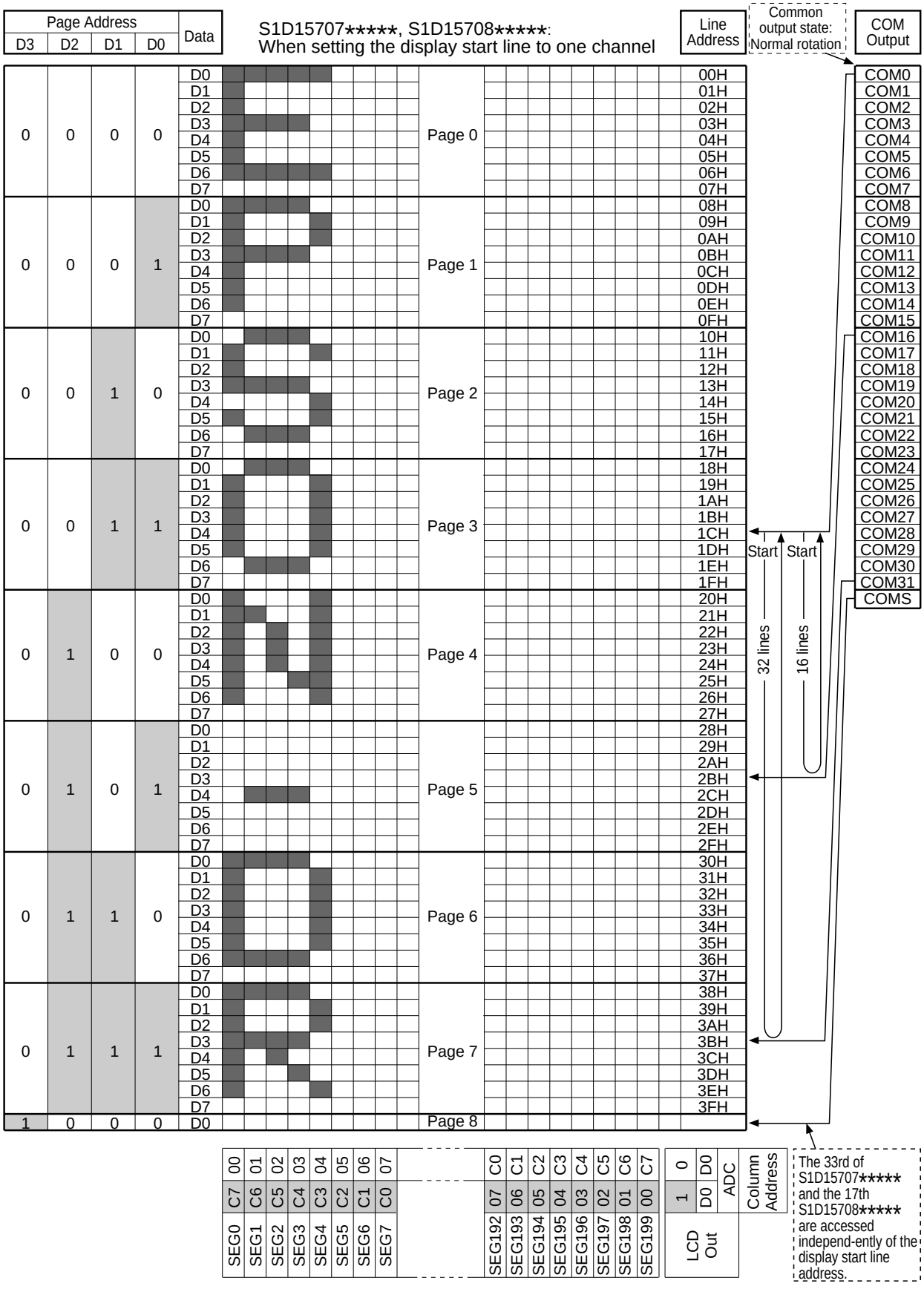

Page Address
D3 D2 D1 D0
Data
S1D15707*****, S1D15708*****:
When setting the display start line to one channel
Line Address
Common output state: Normal rotation
COM Output
Page 0
Page 1
Page 2
Page 3
Page 4
Page 5
Page 6
Page 7
Page 8
Start
Start
32 lines
16 lines
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7
SEG192 SEG193 SEG194 SEG195 SEG196 SEG197 SEG198 SEG199
LCD Out
ADC
Column Address
The 33rd of S1D15707***** and the 17th S1D15708***** are accessed independ-ently of the display start line address.

Fig. 4-2

Display data latch circuit

The display data latch circuit is a latch that temporarily stores the display data output from the display data RAM to the liquid crystal drive circuit.
Since the Display Normal Rotation/Reversal, Display ON/OFF, and Display All Lighting ON/OFF commands control the data in this latch, the data within the display data RAM is not changed.

Oscillator Circuit

This oscillator circuit is a CR type oscillator and generates display clocks. The oscillator circuit is valid only when M/S=HIGH and CLS=HIGH and starts oscillation after the Built-in Oscillator Circuit ON command is entered. When CLS=LOW, the oscillation is stopped and the display clocks are entered from the CL pin.

Display Timing Generator Circuit

This display timing generator circuit generates timing signals from the display clocks to the line address circuit and the display latch circuit. It latches the display data to the display data latch circuit and outputs it to the segment drive output pin by synchronizing to the display clocks. The read operation of display data to the liquid crystal drive circuit is completely independent of the access to the display data RAM from the MPU. Therefore even when the display data RAM is asynchronously accessed during liquid crystal display, the access will not have any adverse effect on the display such as flickering.
The circuit also generates the internal common timing, liquid crystal alternating current signal (FR), and synchronous signal (SYNC) from the display clocks.
As shown in Fig. 5 and 6, the FR normally generates the drive waveforms in the 2-frame alternating current drive system to the liquid crystal drive circuit. It can generate n-line reversal alternating current drive waveforms by setting data (n-1) to the n-line reversal drive register. If a display quality problem such as crosstalk occurs, it can be improved by using the n-line reversal alternating current drive waveforms. Determine the number of lines (n) to which alternating current is applied by actually displaying the liquid crystal.
SNYC is a signal that synchronizes the line counter and common timing generator circuit to the SYNC signal output side IC. Therefore the SYNC signal becomes a waveform at a duty ratio of 50% that synchronizes to the frame synchronization.
When the S1D15705 series is used for the multiple chip configuration, the slave side needs to supply the display timing signals (FR, SYNC, CL, and $\overline{DOF}$) from the master side.
Table 5 shows the state of FR, SYNC, CL, or $\overline{DOF}$.

Table 5

Operation mode		FR	SYNC	CL	DOF
Master (M/S=HIGH)	Built-in oscillator circuit valid (CLS=HIGH)	Output	Output	Output	Output
	Built-in oscillator circuit invalid (CLS=LOW)	Output	Output	Input	Output
Slave (M/S=LOW)	Built-in oscillator circuit valid (CLS=HIGH)	Input	Input	Input	Input
	Built-in oscillator circuit invalid (CLS=LOW)	Input	Input	Input	Input

2-frame alternating current drive waveforms

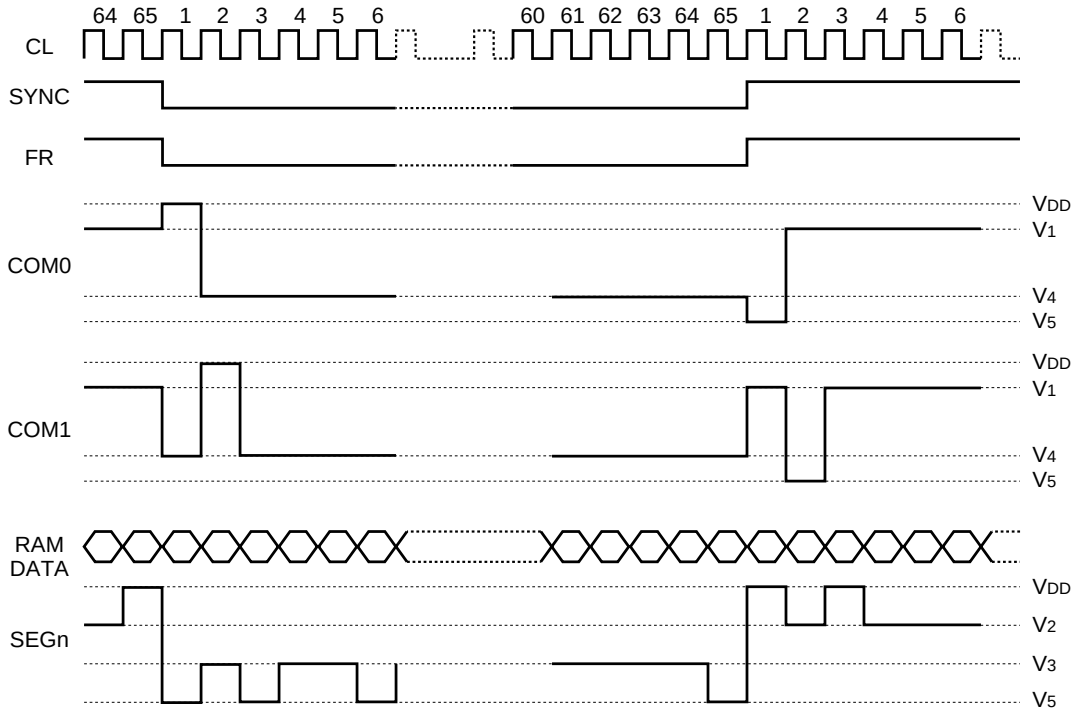


Fig. 5

n-line reversal alternating current drive waveforms (Example of n=5: when the line reversal register is set to 4)

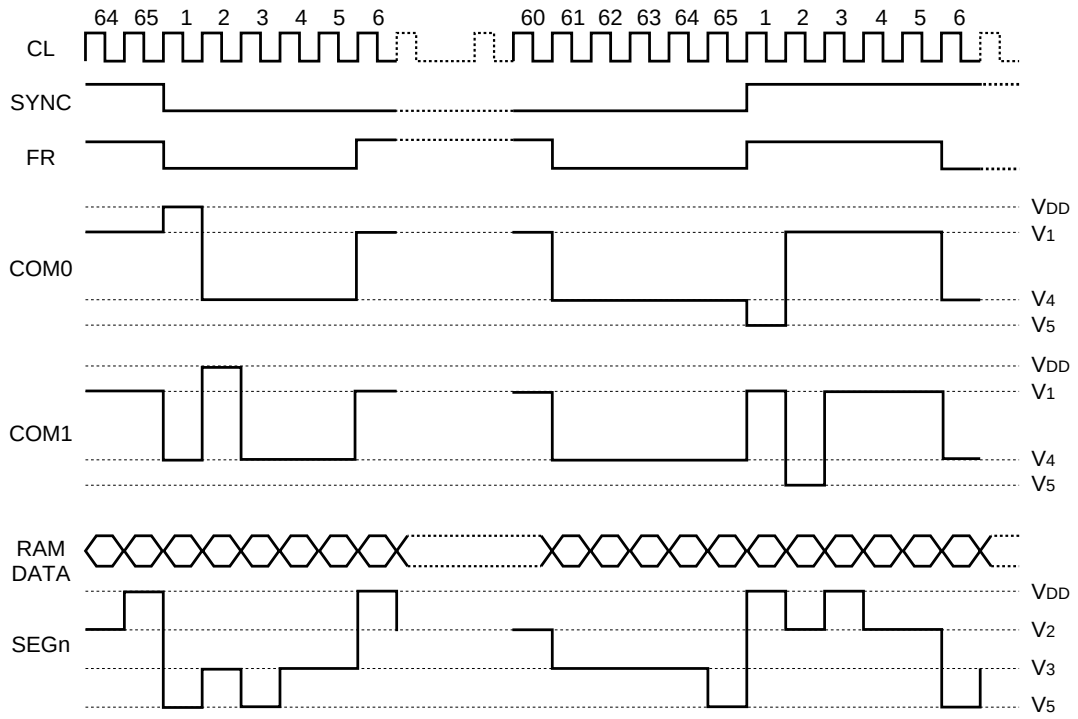


Fig. 6

Common Output State Selection Circuit

The S1D15705 series can set the scanning direction of the COM output using the common output state selection command (see Fig. 6). Therefore the IC assignment restrictions at LCD module assembly are reduced.

Table 6

State	COM scanning direction		
	S1D15705***	**S1D15707*****	**S1D15708*****
Normal rotation	COM 0 → COM 63	COM 0 → COM 31	COM 0 → COM 15
Reversal	COM 63 → COM 0	COM 31 → COM 0	COM 15 → COM 0

Liquid Crystal Drive Circuit

These are a 233-channel (S1D15705***** and S1D15707*****), a 217-channel (S1D15708*****) multiplexers that generate four voltage levels for liquid crystal drive. It outputs the liquid crystal drive voltage that corresponds to the combinations of the display data, COM scanning signal, and FR signal.
Fig. 7 shows examples of the SEG and COM output waveforms.

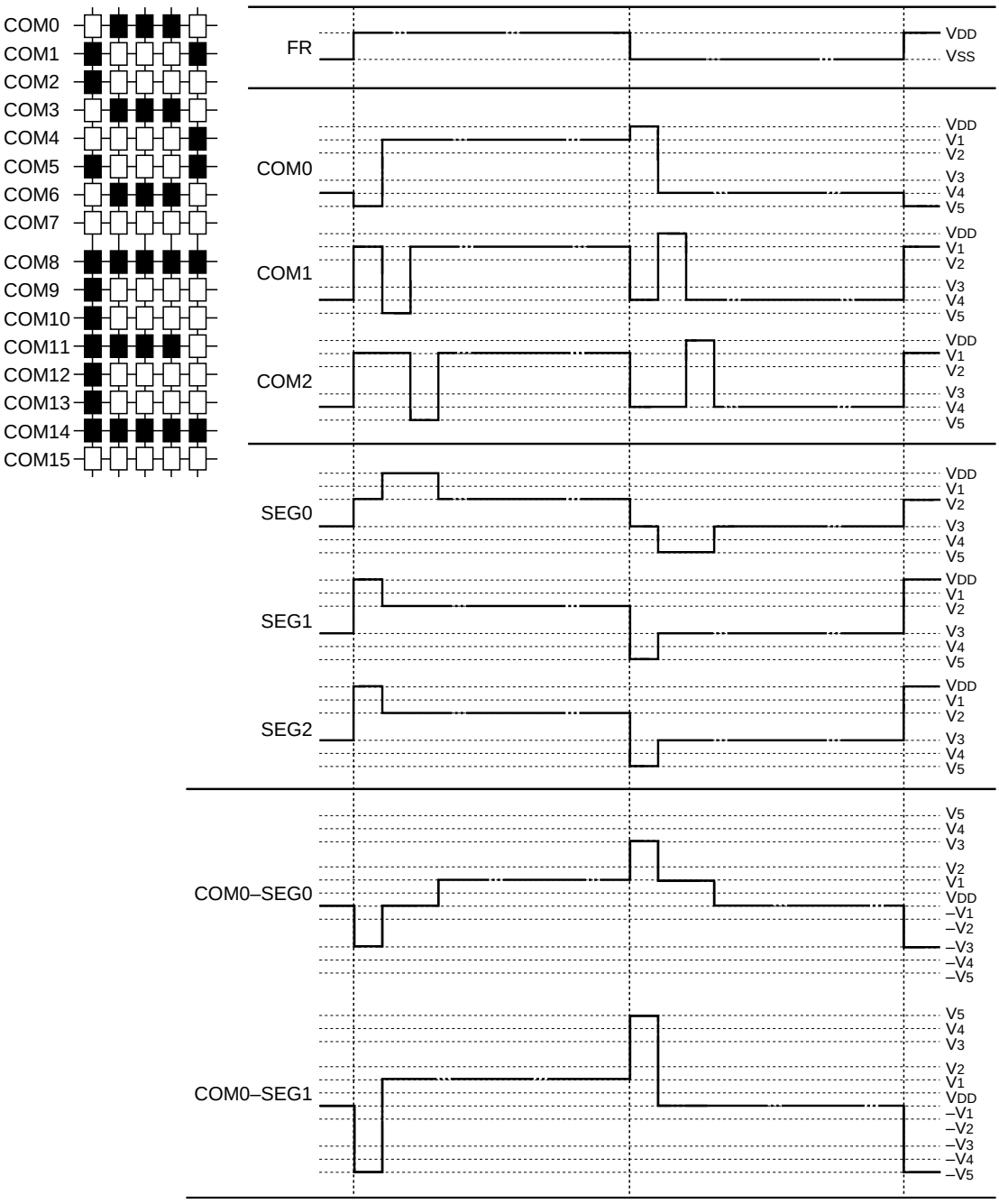

COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
SEG0
SEG1
SEG2
VDD
V1
V2
V3
V4
V5
COM0–SEG0
COM0–SEG1
–V1
–V2
–V3
–V4
–V5

Fig. 7

Power Supply Circuit

This power supply circuit is a low power supply consumption one that generates the voltage required for the liquid crystal drive and consists of a boosting circuit, voltage adjusting circuit, and voltage follower circuit. It is valid only at master operation.
The power supply circuit ON/OFF controls the boosting circuit, voltage adjusting circuit, and voltage follower circuit using the power supply control set command, respectively.
Therefore, it can also use the partial functions of the external power supply and built-in power supply together. Table 7 lists the functions that control 3-bit data using the power control set command and Table 8 lists the reference combinations.

Table 7 Description of controlling bits using the power control set command

Item		State "1"	State "0"
D2	Boosting circuit control bit	ON	OFF
D1	Voltage adjusting circuit (V adjusting circuit) control bit	ON	OFF
D0	Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table 8 Reference combinations

Status of use	D2	D1	D0	Boosting circuit	V adjusting circuit	V/F circuit	External voltage input	Boosting system pin
① Built-in power supply used	1	1	1	O	O	O	V_{SS2}	Used
② V adjusting circuit and V/F circuit only	0	1	1	X	O	O	V_{OUT}, V_{SS2}	OPEN
③ V/F circuit only	0	0	1	X	X	O	V_5, V_{SS2}	OPEN
④ External power supply only	0	0	0	X	X	X	V_1 to V_5	OPEN

- The boosting system pin indicates the CAP1+, CAP1–, CAP2+, CAP2–, or CAP3– pin.
- Although the combinations other than those listed in the above table are also possible, they cannot be recommended because they are not actual use methods.

Boosting circuit

The boosting circuit incorporated in the S1D15705 series enables the quadruple boosting, triple boosting, and double boosting of the V_{DD} – V_{SS2} potential.
For the quadruple boosting, the V_{DD} ↔ V_{SS2} potential is quadruple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔and CAP1–, between CAP2+↔ and CAP2–, between CAP1+↔ and CAP3–, and between V_{SS2}↔ and V_{OUT}.
For the triple boosting, the V_{DD} ↔ V_{SS2} potential is triple-boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, between CAP2+↔ and CAP2–, and between V_{SS2}↔ and V_{OUT} and strapping both CAP3– and V_{OUT} pins.
For the double boosting, the V_{DD} ↔ V_{SS2} potential is doubly boosted to the negative side and output to the V_{OUT} pin by connecting the capacitor C1 between CAP1+↔ and CAP1–, and between V_{SS2}↔, setting CAP2+ to OPEN, and V_{OUT} and strapping CAP2–, CAP3–, and V_{OUT} pins.
Fig. 8 shows the relationships of boosting potential.

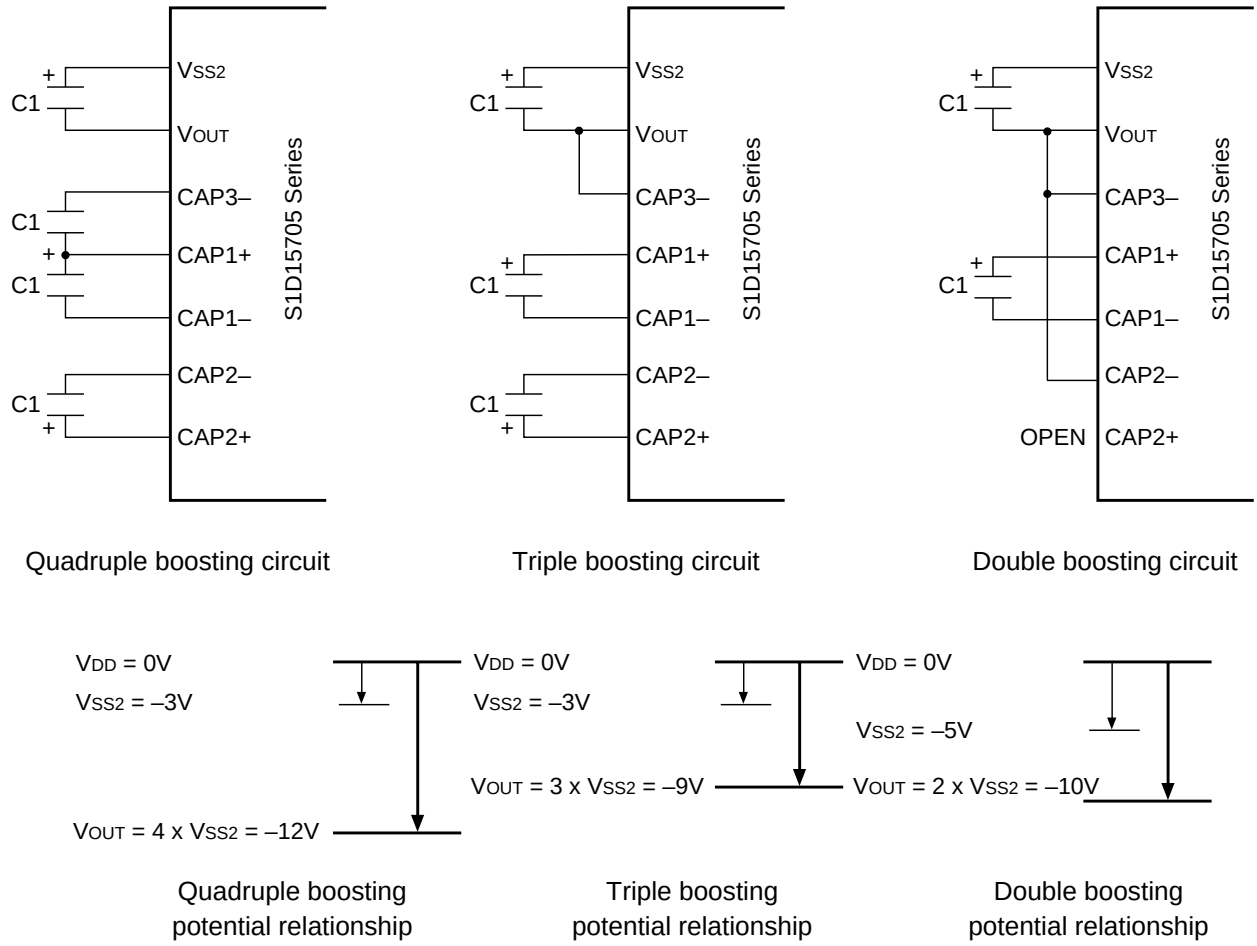


Fig. 8

- Set the VSS2" voltage range so that the voltage of the VOUT pin cannot exceed the absolute maximum ratings.

Voltage adjusting circuit

The boosting voltage generated in VOUT outputs the liquid crystal drive voltage V5 through the voltage adjusting circuit.
Since the S1D15705 series incorporates a high-accuracy constant power supply, 64-step electronic control function, and V5 voltage adjusting resistor, a high-accuracy voltage adjusting circuit can eliminate and save parts.

(A) When using the V5 voltage adjusting built-in resistor
The liquid crystal power supply voltage V5 can be controlled only using the command without an external resistor and the light and shade of liquid crystal display be adjusted by using the V5 voltage adjusting built-in resistor and the electronic control function.
The V5 voltage can be obtained according to Expression A-1 within the range of |V5|<|VOUT|.

$$V_5 = \left(1+\frac{Rb}{Ra}\right)\cdot V_{EV} = \left(1+\frac{Rb}{Ra}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression A-1)}$$

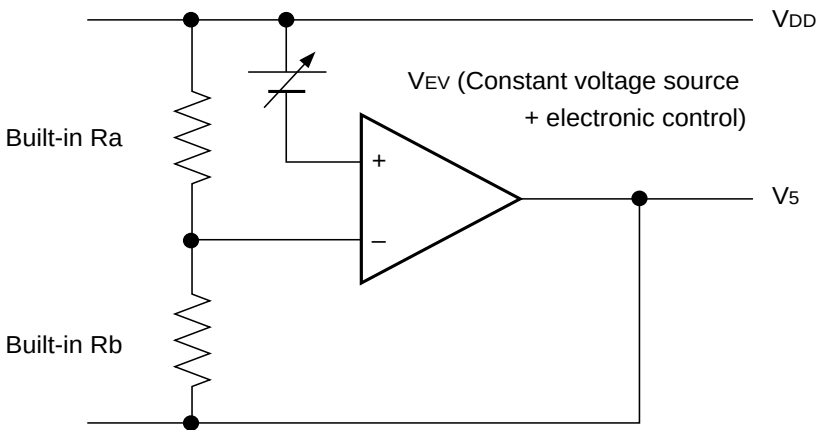


Fig. 9

VREG is a constant voltage source within an IC, and the value at Ta=25°C is constant as listed in Table 9.

Table 9

Device	Temperature gradient	Unit	VREG	Unit
Internal power supply	–0.05	[%/°C]	–2.1	[V]

α indicates an electronic control command value. Setting data in a 6-bit electronic control register enters one state among 64 states. Table 10 lists the values of α based on the setup of the electronic control register.

Table 10

D5	D4	D3	D2	D1	D0	α
0	0	0	0	0	0	63
0	0	0	0	0	1	62
0	0	0	0	1	0	61
			⋮			⋮
1	1	1	1	0	1	2
1	1	1	1	1	0	1
1	1	1	1	1	1	0

Rb/Ra indicates the V5 voltage adjusting built-in resistance ratio and can be adjusted into eight steps using the V5 voltage adjusting built-in resistance ratio set command. The reference values of the (1+Rb/Ra) ratio are obtained as listed in Table 11 by setting 3-bit data in the V5 voltage adjusting built-in resistance ratio register.

Table 11 (Reference values)

Register			S1D15705*****	S1D15707***** / S1D15708*****
			Device per temperature gradient [Unit: %/°C]	Device per temperature gradient [Unit: %/°C]
D2	D1	D0	–0.05	–0.05
0	0	0	4.5	3.0
0	0	1	5.0	3.5
0	1	0	5.5	4.0
0	1	1	6.0	4.5
1	0	0	6.5	5.0
1	0	1	7.0	5.5
1	1	0	7.6	6.0
1	1	1	8.1	6.5

It is necessary to take a manufacturing deviation of upto ±7% of the built-in resistance ratio into consideration. When this is not permissible, supplement external Ra and Rb to ajdust the V5 voltage.
Figs. 10 show the V5 voltage reference values per temperature gradient device based on the values of the V5 voltage adjusting built-in resistance ratio register and electronic control register at Ta=25°C.

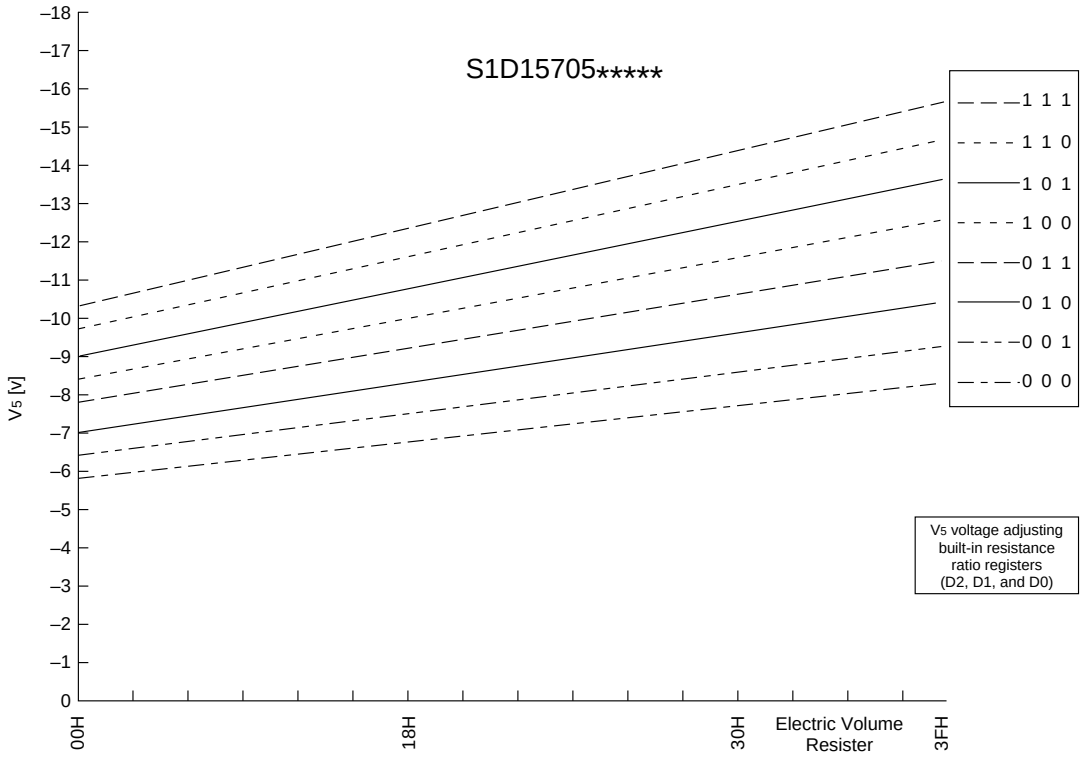


Fig. 10-1 S1D15705***** Temperature gradient = –0.05%/°C device

V_5 voltage based on the values of V_5 voltage adjusting built-in resistance ratio register and electronic control register

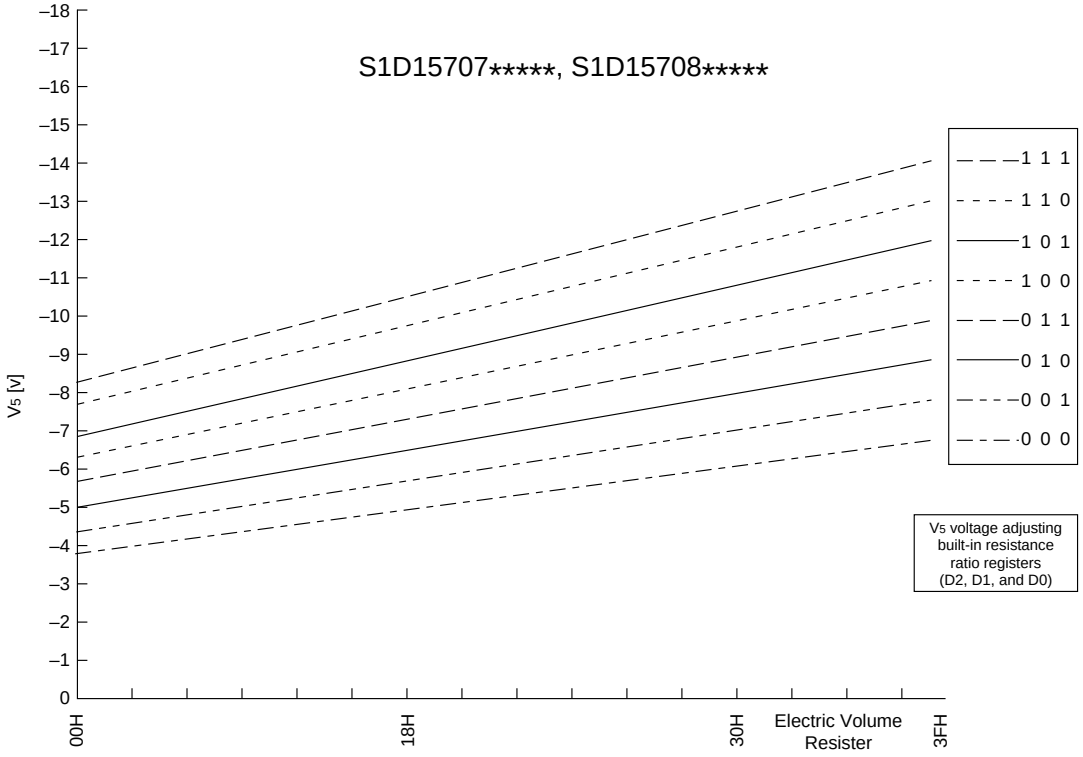


Fig. 10-2 S1D15707*****, S1D15708***** Temperature gradient = –0.05%/°C device

V_5 voltage based on the values of V_5 voltage adjusting built-in resistance ratio register and electronic control register
*S1D15708 should be used in system operating voltage ranges. (V_5–V_{DD} = –10V or V_5–V_{DD}=less than –10V)

<Setting example: S1D15705★★★★★ When setting V_5 = –9 V at Ta=25°C>
From Fig. 8 and Expression A-1.

Table 12

Description	Register					
	D5	D4	D3	D2	D1	D0
V_5 voltage adjusting	–	–	–	0	1	0
electronic control	0	1	1	0	0	1

In this case, Table 13 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 13

V_5	Min.		Typ.		Max.	Unit
Variable range	–11.6	to	–9.3	to	–7.1	[V]
Pitch width			67			[mV]

(B) When using the external resistor (not using the V_5 voltage adjusting built-in resistor) ①
The liquid crystal power supply voltage V_5 can also be set by adding the resistors (Ra' and Rb') between V_{DD} and V_R and between V_R and V_5 without the V5 voltage adjusting built-in resistor (IRS pin=LOW). Also in this case, the liquid crystal power supply voltage V_5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V_5 voltage can be obtained from Expression B-1 by setting the external resistors Ra' and Rb' within the range of $|V_5| < |V_{OUT}|$.

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot V_{EV} = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \quad \left[\because V_{EV} = \left(1-\alpha/162\right)\cdot V_{REG}\right] \qquad \text{(Expression B-1)}$$

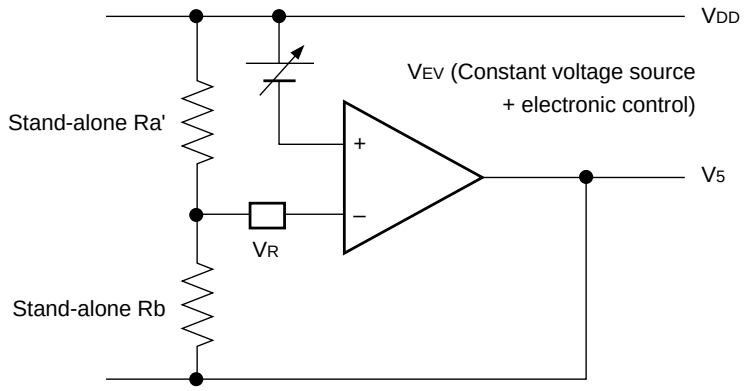


Fig. 11

<Setting example: S1D15705★★★★★ When setting V_5=–7 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$
$$V_{REG} = -2.1V$$

From Expression B-1, it follows that

$$V_5 = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{\alpha}{162}\right)\cdot V_{REG} \qquad \text{(Expression B-2)}$$
$$-7V = \left(1+\frac{Rb'}{Ra'}\right)\cdot\left(1-\frac{31}{162}\right)\cdot(-2.1)$$

Also, suppose the current applied to Ra' and Rb' is 5µA.

$$Ra' + Rb' = 1.4M\Omega \qquad \text{(Expression B-2)}$$

It follows that
Therefore from Expressions B-2 and B-3, we have

$$\frac{Rb'}{Ra'} = 3.12$$
$$Ra' = 340k\Omega$$
$$Rb' = 1060k\Omega$$

In this case, Table 14 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 14

V_5	Min.		Typ.		Max.	Unit
Variable range	–8.6	to	–7.0	to	–5.3	[V]
Pitch width			52			[mV]

(C) When using the external resistor (not using the V_5 voltage adjusting built-in resistor) ②
In the use of the above-mentioned external resistor, the liquid crystal power supply voltage V_5 can also be set by adding the resistors to finely adjust Ra' and Rb'. Also in this case, the liquid crystal power supply voltage V_5 can be controlled using the command and the light and shade of liquid crystal display can be adjusted by using the electronic control function.

The V_5 voltage can be obtained from the following expression C-1 by setting the external resistors R_1, R_2 (variable resistors), and R_3 within the range of $|V_5| < |V_{OUT}|$ and finely adjusting R_2 (ΔR_2).

$$V_5 = \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot V_{EV}$$

$$= \left(1 + \frac{R_3 + R_2 - \Delta R_2}{R_1 + \Delta R_2}\right) \cdot \left(1 - \frac{\alpha}{162}\right) \cdot V_{REG}$$

$$\left[\because V_{EV} = \left(1 - \alpha/162\right) \cdot V_{REG}\right] \quad \text{(Expression C-1)}$$

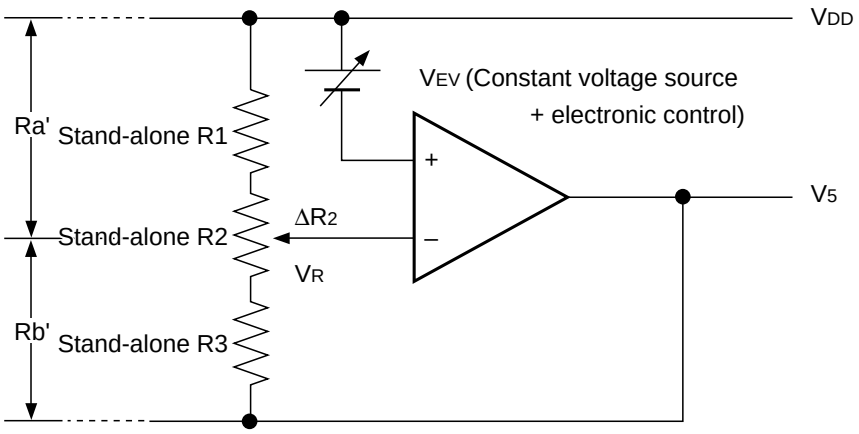


Fig. 12

<Setting example: S1D15705★★★★★ When setting V_5=–5 to –9 V at Ta=25°C>

Set the value of the electronic control register as the intermediate value (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0). From the foregoing we can establish the expression:

$$\alpha = 31$$

$$V_{REG} = -2.1V$$

When ΔR_2=0Ω, to obtain V_5=–9 V from Expression C-1, it follows that

$$-9V = \left(1 + \frac{R_3 + R_2}{R_1}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Expression C-2)

When $\Delta R_2 = R_2$, to obtain V_5=-5V, it follows that

$$-5V = \left(1 + \frac{R_3}{R_1 + R_2}\right) \cdot \left(1 - \frac{31}{162}\right) \cdot (-2.1)$$

(Expression C-3)

Also, suppose the current applied between V_{DD} and V_5 is 5μA.

$$R_1 + R_2 + R_3 = 1.4M\Omega$$

(Expression C-4)

It follows that
Therefore from Expressions C-2, C-3, and C-4, we have

$$R_1 = 264k\Omega$$

$$R_2 = 211k\Omega$$

$$R_3 = 925k\Omega$$

In this case, Table 6-15 lists the V_5 voltage variable range and pitch width using the electronic control function.

Table 15

V_5	Min.		Typ.		Max.	Unit
Variable range	–8.7	to	–7.0	to	–5.3	[V]
Pitch width			53			[mV]

- When using the V_5 voltage adjusting built-in resistor or electronic control function, the state where at least the voltage adjusting circuit and voltage follower circuit are operated together needs to be set using the power control set command. Also when the boosting circuit is OFF, the voltage needs to be applied from V_{OUT}.
- The V_R pin is valid only when the V_5 voltage adjusting built-in resistor (IRS pin=LOW). Set the V_R pin to OPEN when using the V_5 voltage adjusting built-in resistor (IRS pin=HIGH).
- Since the V_R pin has high input impedance, noise must be taken into consideration such as for short and shielded lines.

Liquid crystal voltage generator circuit

The V_5 voltage is resistor-split within an IC and generates the V_1, V_2, V_3, and V_4 potentials required for the liquid crystal drive.
Further, the V_1, V_2, V_3, and V_4 potentials are impedance-converted by the voltage follower and supplied to the liquid crystal drive circuit.
Using the bias set command allows you to select a desired bias ratio from 1/9 or 1/7 for the S1D15705***** and 1/6 or 1/5 for the S1D15707***** and S1D15708***** .

High power mode

The power supply circuit incorporated in the S1D15705 series has the ultra-low power consumption (normal mode: $\overline{HPM}$=HIGH). Therefore the display quality may be deteriorated in large load liquid crystal or panels. In this case, the display quality can be improved by setting $\overline{HPM}$ pin=LOW (high power mode). Whether to use the power supply circuit in this mode should need the display confirmation by actual equipment.
Besides, if the improvement is insufficient even for the high power mode setting, the crystal liquid drive power needs to be supplied externally.

Command sequence when the built-in power supply is turned off

To turn off the built-in power supply, set it in the power save state and then turn off the power supply according to the command sequence shown in Fig. 13 (procedure).

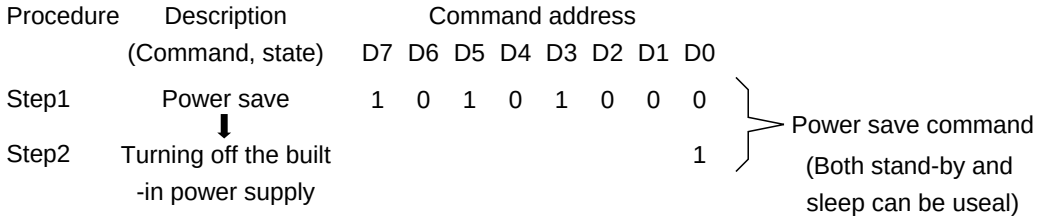
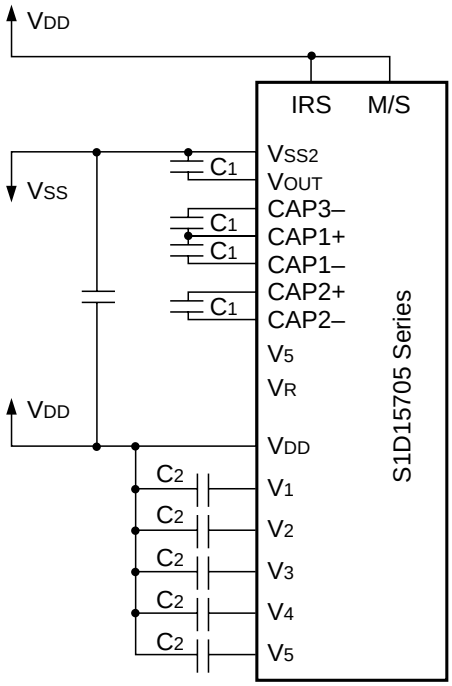


Fig. 13

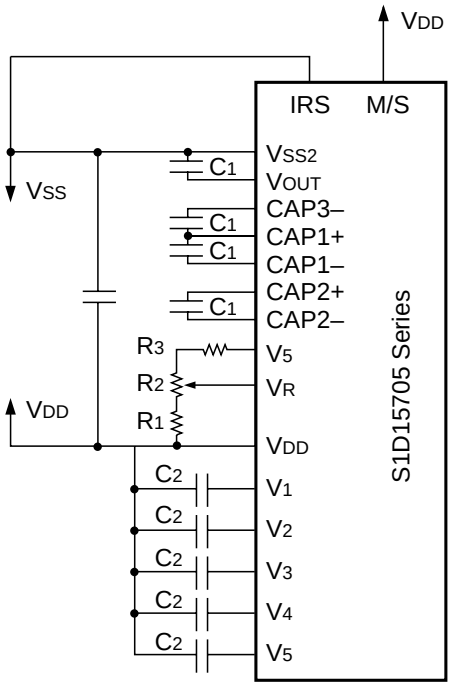
Reference circuit examples

① Built-in power supply used

(1) When using the V_5 voltage adjusting built-in resistor
(Example of V_{SS2}=V_{SS}, quadruple boosting)

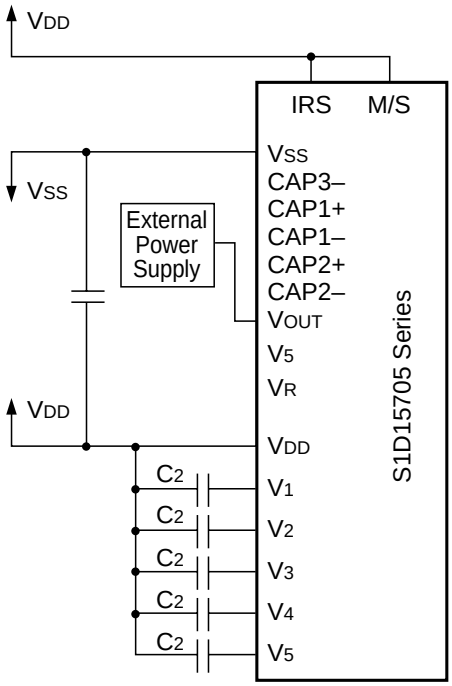


(2) When not using the V_5 voltage adjusting built-in resistor
(Example of V_{SS2}=V_{SS}, quadruple boosting)

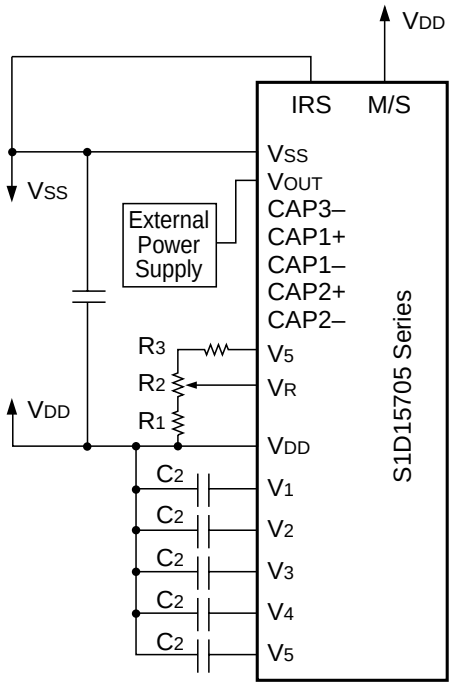


② Only the voltage adjusting circuit and V/F circuit used

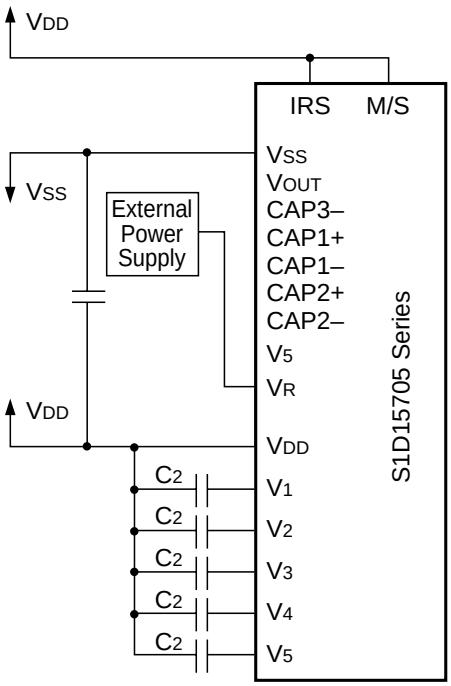
(1) When using the V_5 voltage adjusting built-in resistor



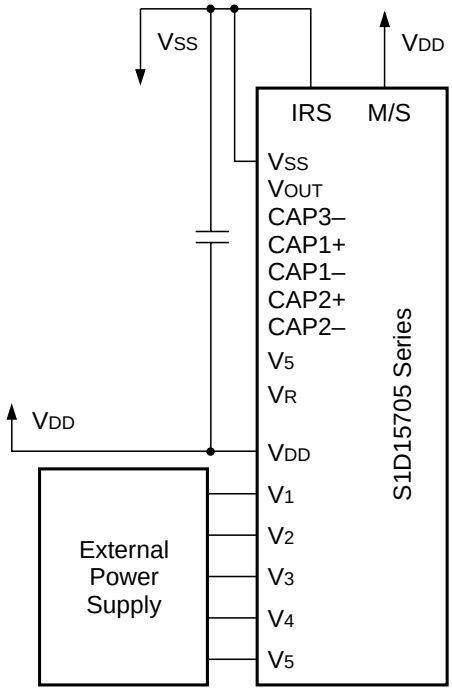
(2) When not using the V_5 voltage adjusting built-in resistor



③ Only the V/F circuit used



④ Only the external power supply used
Depending on all external power supplies



Common reference setting example
At V_5=–8 to –12 V variable

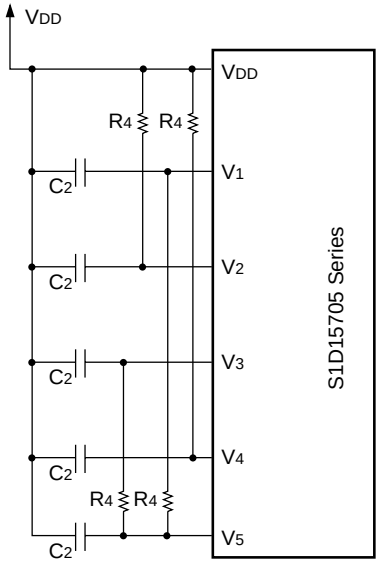
Item	Setting value	Unit
C_1	1.0 to 4.7	µF
C_2	0.01 to 1.0	µF

Fig. 14

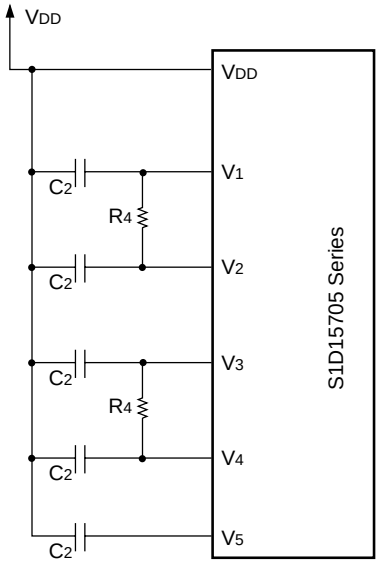
*1 Since the V_R pin has high input impedance, it uses short and shielded wires.
*2 C_1 and C_2 are determined according to the size of the LCD panel. Set a value so that the liquid crystal drive voltage can be stable.
[Setting example] • Turn on the V adjusting circuit and the V/F circuit and apply external voltage.
• Display LCD heavy load patterns like lateral stripes and determine C_2 so that the liquid crystal drive voltages (V_1 to V_5) can be stable.
• Then turn on all built-in power supplies and determine C_1.
*3 Capacity is connected in order to stabilize voltage between V_{DD} and V_{SS} power supplies.

*4 When the built-in V/F circuit is used to drive an LCD panel with heavy alternating or direct current load, we recommend that external resistance be connected in order to stabilize V/F outputs, or electric potentials, V_1, V_2, V_3 and V_4.

Exemplary connection diagram 1 for external resistance



Exemplary connection diagram 2 for external resistance



Adjust resistance value R_4 to the optimal level by checking driving waveform displayed on the LCD.

Reference setting: R_4 = 0.1 to 1.0 [MΩ]

Fig. 15

*5 Precautions when installing the COG

When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display.
Therefore, when installing the COG design the module paying sufficient considerations to the following three points.

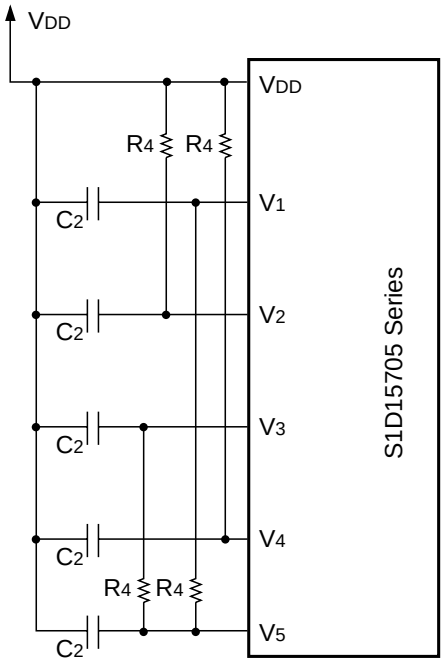
1. Suppress the resistance occurring between the driver chip pin to the externally connected parts as much as possible.
2. Suppress the resistance connecting to the power supply pin of the driver chip.
3. Make various COG module samples with different ITO sheet resistance to select the module with the sheet resistance with sufficient operation margin.

Also, as for this driver IC, pay sufficient attention to the following points when connecting to external parts for the characteristics of the circuit.

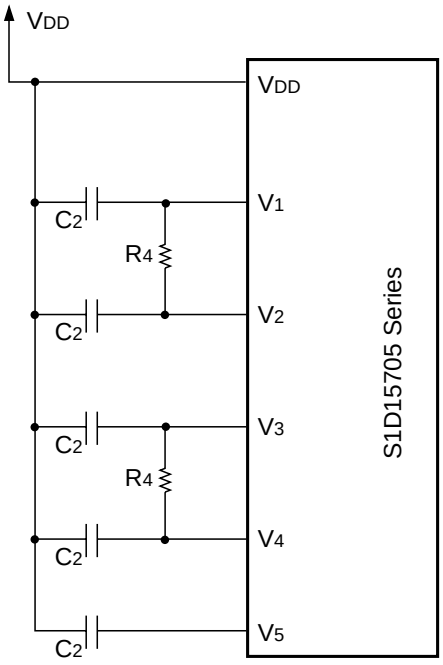
1. Connection to the boosting capacitors The boosting capacitors (the capacitors connecting to respective CAP pins and capacitor being inserted between V_{OUT} and V_{SS2}) of this IC are being switched over by use of the transistor with very low ON-resistance of about 10Ω. However, when installing the COG, the resistance of ITO wiring is being inserted in series with the switching transistor, thus dominating the boosting ability.
   Consequently, the boosting ability will be hindered as a result and pay sufficient attention to the wiring to respective boosting capacitors.
2. Connection of the smoothing capacitors for the liquid crystal drive
   The smoothing capacitors for the liquid crystal driving potentials (V_1. V_2, V_3 and V_4) are indispensable for liquid crystal drives not only for the purpose of mere stabilization of the voltage levels. If the ITO wiring resistance which occurs pursuant to installation of the COG is supplemented to these smoothing capacitors, the liquid crystal driving potentials become unstable to cause non-conformity with the indications of the liquid crystal display. Therefore, when using the COG module, we definitely recommend to connect reinforcing resistors externally.
   Reference value of the resistance is 100kΩ to 1MΩ. Meanwhile, because of the existence of these reinforcing resistors, current consumption will increase.

Indicated below is an exemplary connection diagram of external resistors.
Please make sufficient evaluation work for the display statuses with any connection tests.

Exemplary connection diagram 1.



Exemplary connection diagram 2.



Reset Circuit

When the $\overline{RES}$ input is set to the LOW level, this LSI enters each of the initial setting states

1. Display OFF
2. Display Normal Rotation
3. ADC Select: Normal rotation (ADC command D0=0)
4. Power Control Register: (D2,D1,D0)=(0,0,0)
5. Register Data Clear within Serial Interface
6. LCD Power Supply Bias Ratio:
   S1D15705: 1/9 bias
   S1D15707/S1D15708: 1/6 bias
7. n-Line Alternating Current Reversal Drive Reset
8. Sleeve mode cancel (standby mode is not canceled)
9. Display All Lighting OFF: (Display All Lighting ON/OFF command D0=LOW)
10. Built-in Oscillator Circuit stopped
11. Static Indicator OFF
    Static Indicator Register: (D1,D2)=(0,0)
12. Read Modify Write OFF
13. Display start line set to the first line
14. Column address set to address 0
15. Page address set to page 0
16. Common Output State Normal rotation
17. V_5 Voltage Adjusting Built-in Resistance Ratio Register: (D2,D1,D0)=(0,0,0)
18. Electronic Control Register Set Mode Reset
    Electronic Control Register* (D5, D4, D3, D2, D1, D0) = (1,0,0,0,0,0)
19. n-Line Alternating Current Reversal Register: (D3, D2, D1, D0) = (0, 0, 0, 0)
20. Test Mode Reset

On the other hand, when using the reset command, only the items 11 to 20 of the above-mentioned initial setting are executed.

When the power is turned on, the initialization using the $\overline{RES}$ pin is required. After the initialization using the $\overline{RES}$ pin, each input pin needs to be controlled normally. Besides, when the MPU control signal has high impedance, overcurrent may be applied to an IC. After turning on the power, take action so that the input pin cannot have high impedance.
The S1D15705 Series discharge electric charges of V_5 and V_{OUT} at $\overline{RES}$ pin is set to the LOW level. If external power supplies for driving LCD are used, do not input external power while the $\overline{RES}$ pin is set to the LOW level to prevent short-circuiting between the external power supplies and V_{DD}.

7. COMMAND

The S1D15705 series identifies data bus signals according to the combinations of A0, $\overline{RD}$(E), and $\overline{WR}$(R/$\overline{W}$). Since the interpretation and execution of commands are performed only by the internal timing independently of external clocks, the S1D15705 performs high-speed processing that does not require busy check normally.
The 80 series MPU interface starts commands by inputting low pulses to the $\overline{RD}$ pin at read and to the $\overline{WR}$ pin at write operation. The 68 series MPU interface enters the read state when HIGH is input to the R/$\overline{W}$ pin. It enters the write state when LOW is input to the same pin. It starts commands by inputting high pulses to the E pin (for the timing, see the Timing Characteristics of Chapter 10). Therefore the 68 series MPU interface differs from the 80 series MPU interface in that $\overline{RD}$(E) is set to "1 (H)" at status read and display data read in the Command Description and Command Table. The command description is given below by taking the 80 series MPU interface as an example.
When selecting the serial interface, enter sequential data from D_7.

Command description

(1) Display ON/OFF

This command specifies display ON/OFF.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

For display OFF, the segment and common drivers output the V_{DD} level.

(2) Display Start Line Set

This command specifies the display start line address of the display data RAM shown in Fig. 4. The display area is displayed for 65 lines for the S1D15705*****, 33 lines for the S1D15707***** and 17 lines for the S1D15708***** from the specified line address to the line address increment direction. When this command is used to dynamically change the line address, the vertical smooth scroll and page change are enabled. For details, see the Line address circuit of "Function Description".

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	1	0	0	1	0	0	0	0	0	0	0
					0	0	0	0	0	1	1
					0	0	0	0	1	0	2
							↓				↓
					1	1	1	1	1	0	62
					1	1	1	1	1	1	63

(3) Page Address Set

This command specifies the page address that corresponds to the low address when accessing the display data RAM shown in Fig. 4 from the MPU side. The display data RAM can access desired bits when the page address and column address are specified. Even when the page address is changed, the display state will not be changed. For details, see the Page address circuit of "Function Description".

A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	0	0
							0	0	0	1	1
							0	0	1	0	2
								↓			↓
							0	1	1	1	7
							1	0	0	0	8

(4) Column Address Set

This command specifies the column address of the display data RAM shown in Fig. 4. The column address is set (basically successively) by dividing it into high-order four bits and low-order four bits. Since the column address is automatically incremented by 1 whenever the display data RAM is accessed. The MPU can successively read/write the display data. The column address stops the increment at C7H. In this case, the page address is not changed successively. For details, see the Column address circuit of "Function Description".

	A0	$\overline{E}$ $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
High-order bit →	0	1	0	0	0	0	1	A7	A6	A5	A4
Low-order bit →							0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	0	1	0	0	1	1	0	166
1	0	1	0	0	1	1	1	167
				↓				↓
1	1	0	0	0	1	1	0	198
1	1	0	0	0	1	1	1	199

(5) Status Read

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

BUSY	When BUSY=1, indicates an internal operation being done or reset. The command cannot be accepted until BUSY=0 is reached. However, if the cycle time is satisfied, the command needs not be checked.
ADC	Indicates the correspondence relationship between the column address and segment driver. 0: Reversal (column address 199–n ↔ SEG n) 1: Normal rotation (column address n ↔ SEG n) (Reverses the polarity of ADC command.)
ON/OFF	ON/OFF: Specifies display ON/OFF 0: Display ON 1: Display OFF (Reverses the polarity of display ON/OFF command.)
RESET	Indicates the $\overline{RES}$ signal or that initial setting is being done using the reset command. 0: Operating state 1: Resetting

(6) Display Data Write

This command writes 8-bit data to the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively write the display data.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

(7) Display Data Read

This command reads the 8-bit data in the specified address of the display data RAM. Since the column address is automatically incremented by 1 after the data is written, the MPU can successively read the data consisting of multiple words.
Besides, immediately after the column address is set, dummy read is required one time. For details, see the description of the Display data RAM and internal register access of “Function Description”.
When using the serial interface, the display cannot be read.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

(8) ADC Select (Segment Driver Direction Select)

This command can reverse the correspondence relationship between the column address of the display RAM data shown in Fig. 4 and the segment driver output. Therefore the order of the segment driver output pin can be reversed using the command. After the display data is written and read, the column address is incremented by 1 according to the column address of Fig. 4. For details, see the Column address circuit of "Function Description".

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Clockwise (normal rotation)
										1	Counterclockwise (reversal)

(9) Display Normal Rotation/Reversal

This command can reversal display lighting and non-lighting without overwriting the contents of display data RAM. In this case, the contents of display data RAM are held.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	LCD on potential (normal rotation) RAM data HIGH
										1	LCD on potential (reversal) RAM data LOW

(10) Display All Lighting ON/OFF

This command can forcedly make all display set in the lighting state irrespective of the contents of display data RAM. In this case, the contents of display data RAM are held.
This command has priority over the display normal rotation/reversal command.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display state
										1	Display all lighting

(11) LCD Bias Set

This command selects the bias ratio of the voltage required for liquid crystal drive. The command is valid when the V/F circuit of the power supply circuit is operated.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
											S1D15705*****	S1D15707***** / S1D15708*****
0	1	0	1	0	1	0	0	0	1	0	1/9 bias	1/6 bias
										1	1/7 bias	1/5 bias

(12) Read Modify Write

This command is used together with the end command. Once this command is entered, the column address can be incremented by 1 only using the display data write command instead of being changed using the display read command. This state is held until the end command is entered. When the end command is entered, the column address returns to the address when the read modify write command is entered. This function can reduce the load of the MPU when repeatedly changing data for a specific display area such as a blinking cursor.

A0	$\overline{E}$ RD	R/$\overline{W}$ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* The commands other than Display Data Read/Write can be used even in Read Modify Write mode. However, the column address set command cannot be used.

- Sequence for cursor display

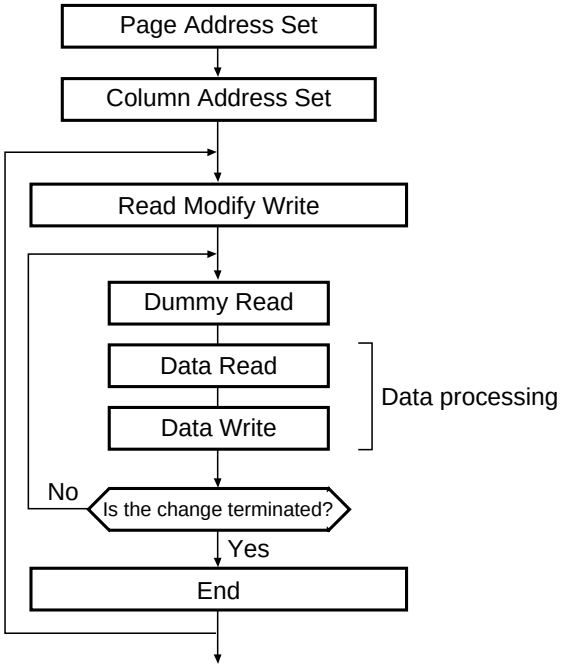


Fig. 16

(13) End

This command resets the Read Modify Write mode and returns the column address to the mode initial address.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

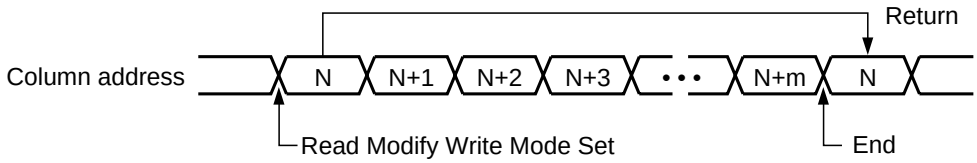


Fig. 17

(14) Reset

This command initializes Display Start Line, Column Address, Page Address, Common Output State, V_5 Voltage Adjusting Built-in Resistance Ratio, Electronic Control, and Static Indicator and resets the Read Modify Write mode and Test mode. This will not have any effect on the display data RAM. For details, see the Reset of " Function Description".
Reset operation is performed after the reset command is entered.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The initialization when the power is applied is performed using the reset signal to the $\overline{RES}$ pin. The reset command cannot be substituted for the signal.

(15) Common Output State Selection

This command can select the scanning direction of the COM output pin. For details, see the Common Output State Selection Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state			
												S1D15705*****	S1D15707*****	S1D15708*****
0	1	0	1	1	0	0	0	*	*	*	Normal rotation	COM0 → COM63	COM0 → COM31	C OM0 → COM15
							1				Reversal	COM63 → COM0	COM31 → COM0	COM15→ COM0

*: Invalid bit

(16) Power Control Set

This command sets the function of the power supply circuit. For details, see the Power Supply Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	1	0			Boosting circuit: OFF
								1			Boosting circuit: ON
									0		V adjusting circuit: OFF
									1		V adjusting circuit: ON
										0	V/F circuit: OFF
										1	V/F circuit: ON

(V/F circuit: Voltage follower circuit, V adjusting circuit: voltage adjusting circuit)

(17) V_5 Voltage Adjusting Built-in Resistance Ratio Set

This command sets the V_5 voltage adjusting built-in resistance ratio. For details, see the Power Supply Circuit of "Function Description".

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb to Ra ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									↓		↓
								1	1	0	
								1	1	1	Large

(18) Electronic Control (2-Byte Command)

This command controls the liquid crystal drive voltage V_5 output from the voltage adjusting circuit of the built-in liquid crystal power supply and can adjust the light and shade of liquid crystal display.
Since this command is a 2-byte command that is used together with the electronic control mode set command and electronic control register set command, always use both the commands consecutively.

• Electronic Control Mode Set
Entering this command validates the electronic control register set command. Once the electronic control mode is set, the commands other than the electronic control register set command cannot be used. This state is reset after data is set in the register using the electronic control register set command.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

• Electronic Control Register Set
This command is used to set 6-bit data in the electronic volume register to allow the liquid crystal drive voltage V_5 to enter one-state voltage value among 64-state voltage values.
After this command is entered and the electronic control register is set, the electronic control mode is reset.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	| V5 |
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	0	1	
0	1	0	*	*	0	0	0	0	1	0	
							↓				↓
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

*: Invalid bit

When not using the electronic control function, set (1,0,0,0,0,0).

• Sequence of the electronic control register set

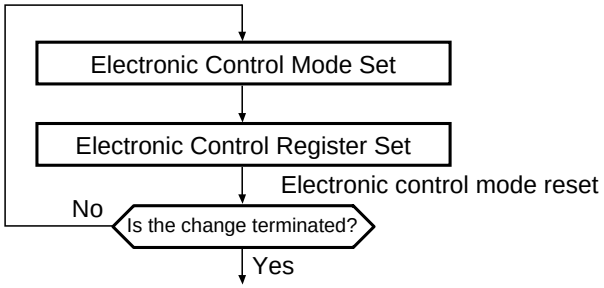


Fig. 18

(19) Static Indicator (2-Byte Command)

This command controls the indicator display of the static drive system. The static indicator display is controlled only using this command, and this command is independent of other display control commands.
The static indicator is used to connect the SYNC pin to one of its liquid crystal drive electrodes and the FRS pin to the other. For the electrodes used for the static indicator, the pattern separated from the electrodes for dynamic drive are recommended. When this pattern is too adjacent, the deterioration of liquid crystal and electrodes may be caused.
Since the static indicator ON command is a 2-byte command that is used together with the static indicator register set command, always use both the commands consecutively. (The static indicator OFF command is a 1-byte command.)

• Static Indicator ON/OFF

Entering the static indicator ON command validates the static indicator register set command. Once the static indicator ON command is entered, the commands other than the static indicator register set command cannot be used. This state is reset after the data is set in the register using the static indicator register set command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Static indicator
0	1	0	1	0	1	0	1	1	0	0	OFF
										1	ON

• Static Indicator Register Set

This command sets data in the 2-bit static indicator register and sets the blinking state of the static indicator.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Indicator display state
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinks at an interval of approximately 0.5 second.)
									1	0	ON (blinks at an interval of approximately one second.)
									1	1	ON (goes on at all times.)

*: Invalid bit

• Sequence of Static Indicator Register Set

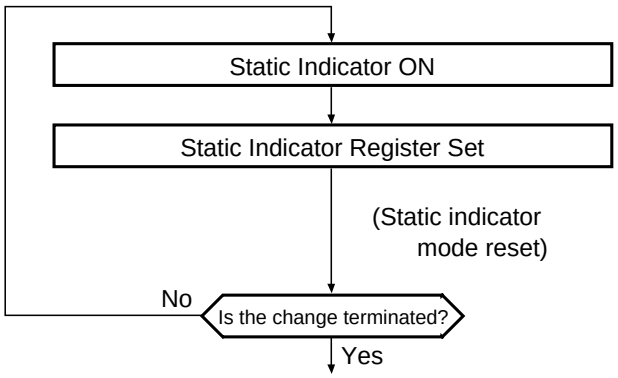


Fig. 19

(20) Power Save

This command makes the static indicator enter the power save state and can greatly reduce the power consumption. The power save state consists of the sleep state and stand-by state.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Power save state
0	1	0	1	0	1	0	1	0	0	0	Stand-by state
										1	Sleep state

The operating state before the display data and power save activation is held in the sleep and stand-by states, and the display data RAM can also be accessed from the MPU.

• Sleep State

This command stops all the operations of LCD display systems, and can reduce the power consumption approximate to the static current when they are not accessed from the MPU. The internal state in the sleep state is as follows:

(1) The oscillator circuit and the LCD power supply circuit are stopped.
(2) All liquid crystal drive circuit is stopped and the segment and common drivers output the V_{DD} level.

• Stand-by State

This command stops the operation of the duty LCD display system and operates only the static drive system for indicators. Consequently the minimum current consumption required for the static drive is obtained. The internal state in the stand-by state is as follows:

(1) The LCD power supply circuit is stopped. The oscillator circuit is operated.
(2) The duty drive system liquid crystal drive circuit is stopped and the segment and common drivers output the V_{DD} level. The static drive system is operated.
    * When using external power supplies, it is recommended that the function of the external power supply circuit should be stopped at power save activation. For example, when providing each level of the liquid crystal drive voltage using a stand-alone split resistor circuit, it is recommended that the circuit which cuts off the current applied to the split resistor circuit should be added at power save activation. The S1D15705 series has the liquid crystal display blanking control pin $\overline{DOF}$ and is set to LOW at power save activation. The function of the external power supply circuit can be stopped using the $\overline{DOF}$ output.

(21) Power Save Reset

This command resets the power save state and returns the state before power save activation.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	1

(22) n-Line Reversal Drive Register Set

This command sets the number of reversal lines of the liquid crystal drive in the register. 2 to 16 lines can be set. For details, see the Display Timing Generator Circuit of “Function Description”.

A0	E RD	R/W WR	D7	D6	D5	D4	D3	D2	D1	D0	Line of reversal lines
0	1	0	0	0	1	1	0	0	0	0	—
							0	0	0	1	2
							0	0	1	0	3
									↓		↓
							1	1	1	0	15
							1	1	1	1	16

(23) n-Line Reversal Drive Reset

This command resets the n-line reversal alternating current drive and returns to the normal 2-frame reversal alternating current drive system. The value of the n-line reversal alternating current drive register is not changed.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	0	0

(24) Built-in Oscillator Circuit ON

This command starts the operation of the built-in CR oscillator circuit. This command is valid only for the master operation (M/S=HIGH) and built-in oscillator circuit valid (CLS=HIGH).

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	1	1

(25) NOP

Non-OPeration

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

(26) Test

IC chip test command. Do not use this command. If the test command is used incorrectly, it can be reset by setting the $\overline{RES}$ input to LOW or by using the reset command or NOP.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

(Note) Although the S1D15705 series holds the command operating state, it may change the internal state if excessive foreign noise is entered. Such action that suppresses the generation of noise and prevents the effect of noise needs to be taken on installation and systems. Besides, to prevent sudden noise, it is recommended that the operating state should periodically be refreshed.

Table 16 S1D15705 Series Commands

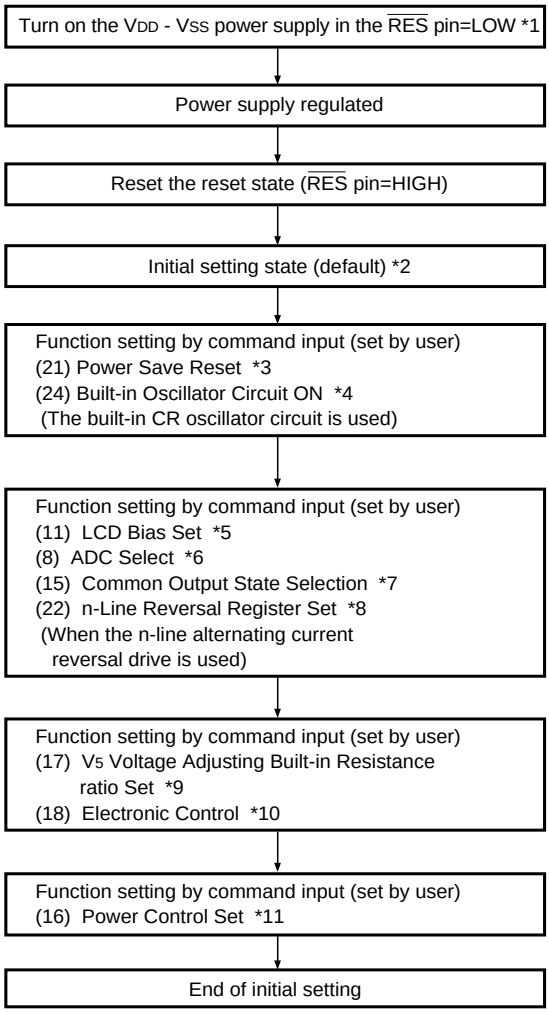
Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display Start Line Set	0	1	0	0	1	Display start address						Sets the display start line address of the display RAM.
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display RAM.
(4) Column Address Set High-Order Bit	0	1	0	0	0	0	1	High order Column address				Sets the high-order four bits of the column address of the display RAM.
Column Address Set Low-Order Bit	0	1	0	0	0	0	0	Low order Column address				Sets the low-order four bits of the column address of the display RAM.
(5) Status Read	0	0	1	Status				0	0	0	0	Reads the status information.
(6) Display Data Read	1	1	0	Write data								Writes data on the display RAM.
(7) Display Data Write	1	0	1	Read data								Reads data from the display RAM.
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0/1	Supports the SEG output of the display RAM address. 0: normal rotation, 1: Reversal
(9) Display Normal Rotation/Reversal	0	1	0	1	0	1	0	0	1	1	0/1	LCD display normal rotation/ reversal 0: normal rotation, 1: Reversal
(10) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Display all lighting 0: normal display, 1: All ON
(11) LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0/1	Sets the LCD drive voltage bias ratio. S1D15705★★★★★ 0: 1/9, 1: 1/7, S1D15707★★★★★ 0: 1/6, 1: 1/5
(12) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. At write operation: By 1, at read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Resets Read Modify Write.
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal resetting
(15) Common Output State Selection	0	1	0	1	1	0	0	0/1	*	*	*	Selects the scanning direction of the COM output. 0: Normal rotation, 1: Reversal
(16) Power Control Set	0	1	0	0	0	1	0	1	Operating state			Selects the state of the built-in power supply
(17) V_5 Voltage Adjusting Internal Resistance Ratio Set	0	1	0	0	0	1	0	0	Resistance ratio setting			Selects the state of the built-in resistance ratio (Rb/Ra).
(18) Electronic Control Mode Set	0	1	0	1	0	0	0	0	0	0	1	
Electronic Control Register Set	0	1	0	*	*	Electronic control value						Sets the V_5 output voltage in the electronic register.
(19) Static Indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0/1	0: OFF, 1: ON
Static Indicator Register Set	0	1	0	*	*	*	*	*	*	State		Sets the blinking state.
(20) Power Save	0	1	0	1	0	1	0	1	0	0	0/1	Moves to the power save state. 0: Stand-by, 1: Sleep
(21) Power Save Reset	0	1	0	1	1	1	0	0	0	0	1	Resets power save.
(22) n-Line Reversal Drive Register Set	0	1	0	0	0	1	1	Number of reversal Line				Sets the number of line reversal drive lines.
(23) n-Line Reversal Drive Reset	0	1	0	1	1	1	0	0	1	0	0	Resets the line reversal drive.
(24) Built-in Oscillator Circuit ON	0	1	0	1	0	1	0	1	0	1	1	Starts the operation of the built-in CR oscillator circuit.
(25) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-Operation command
(26) Test	0	1	0	1	1	1	1	*	*	*	*	Do not use the IC chip test command.

*: Invalid bit

8. COMMAND SETTING

Instruction Setup: Reference

(1) Initial Setting



Notes: Reference items

*1: If external power supplies for driving LCD are used, do not supply voltage on VOUT or V5 pin during the period when RES = LOW. Instead, input voltage after releasing the reset state.
6. Function Description "Reset Circuit"

*2: The contents of DDRAM are not defined even in the initial setting state after resetting.
6. Function Description Section "Reset Circuit"

*3: 7. Command Description Item (21) Power save reset

*4: 7. Command Description Item (24) Built-in oscillator circuit ON

*5: 7. Command Description Item (11) LCD bias set

*6: 7. Command Description Item (8) ADC select

*7: 7. Command Description Item (15) Common output state selection

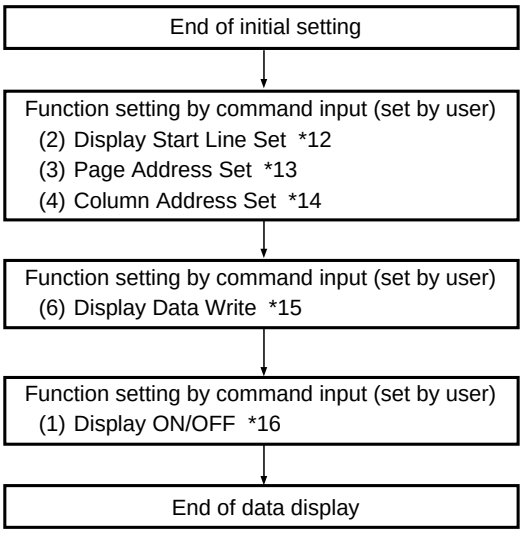
*8: 6. Function Description Section "Display Timing Generator Circuit", 7. Command Description Item (22) n-Line Reversal Register Set

*9: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (17) V5 Voltage Adjusting Built-in Resistance ratio Set

*10: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (18) Electronic Control

*11: 6. Function Description Section "Power Supply Circuit" and 7. Command Description Item (16) Power Control Set

(2) Data Display



Notes: Reference items

*12: 7. Command Description Item (2) Display Start Line Set

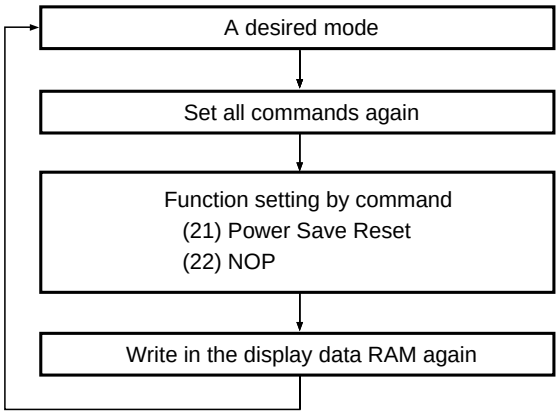
*13: 7. Command Description Item (3) Page Address Set

*14: 7. Command Description Item (4) Column Address Set

*15: The contents of DDRAM is not defined after completing initial setting. Enter data in each DDRAM to be used for display.
7. Command Description Item (6) Display Data Write

*16: Avoid activating the display function with entering space characters as the data if possible.
7. Command Description Item (1) Display ON/OFF

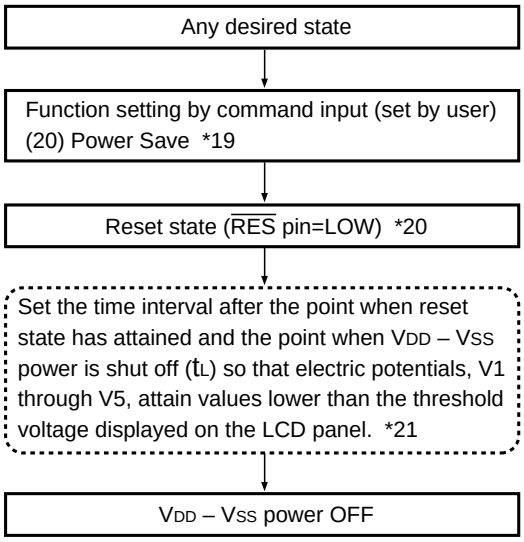
(3) Refresh *17



Notes: Reference items

*17: It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.
Input (21) Power Save Reset and (22) NOP in order to avoid going into a power save state and IC tip test state accidentally.

(4) Power OFF *17



Notes: Reference items

*18: This IC is a $V_{DD} – V_{SS}$ power system circuit controlling the LCD driving circuit for the $V_{DD} – V_5$ power system. Shutting of power with voltage remaining in the $V_{DD} – V_5$ power system may cause uncontrolling voltage to be output from the SEG and COM pins. Follow the Power OFF sequence.

*19: 7. Command Description Item Power Saving

*20: When external power supplies for driving LCD are used, turn all external power supplies off before entering reset state.
6. Function Description Item Reset Circuit

*21: The reference value for the threshold voltage of the LCD panel is 1 [V].
When the built-in power circuit is used, the discharge time, t_H, or the time interval between the point when the reset state has started and the point when voltage between V_{DD} and V_5 becomes 1 [V] depends on the $V_{DD} – V_{SS}$ power voltage and the capacity C2 connected between $V_1 – V_5$ and V_{DD}.

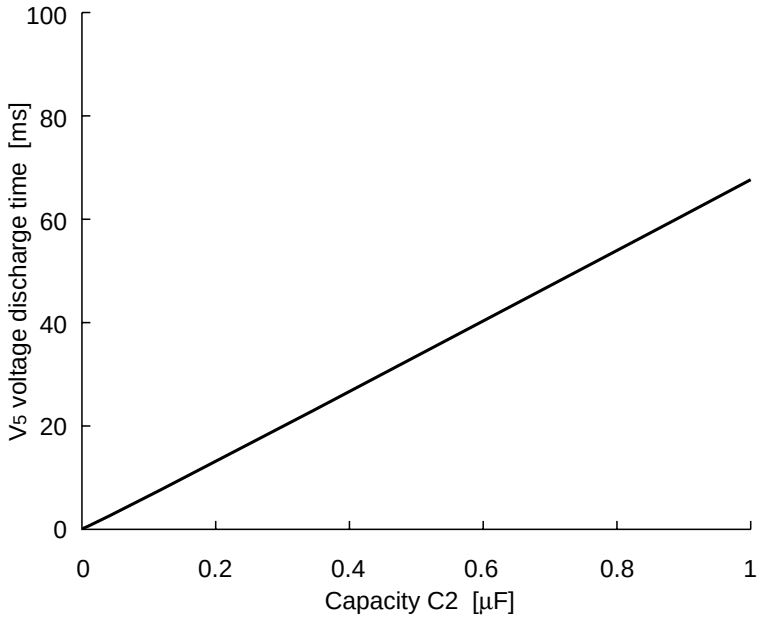


Fig. 20

Set up t_L so that the relationship, $t_L > t_H$, is maintained. A state of $t_L < t_H$ may cause faulty display.

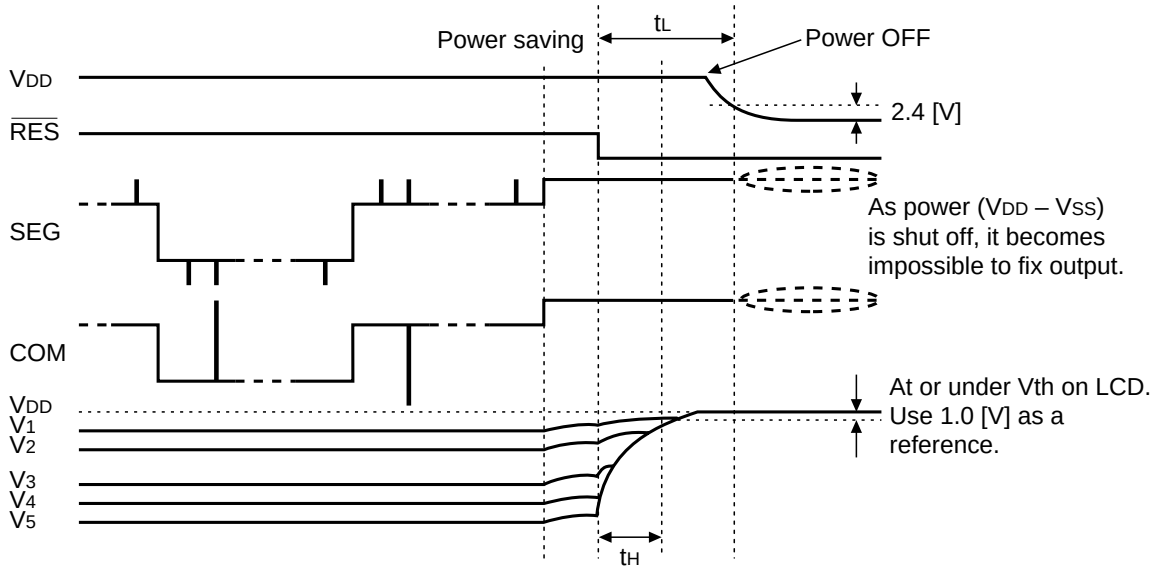
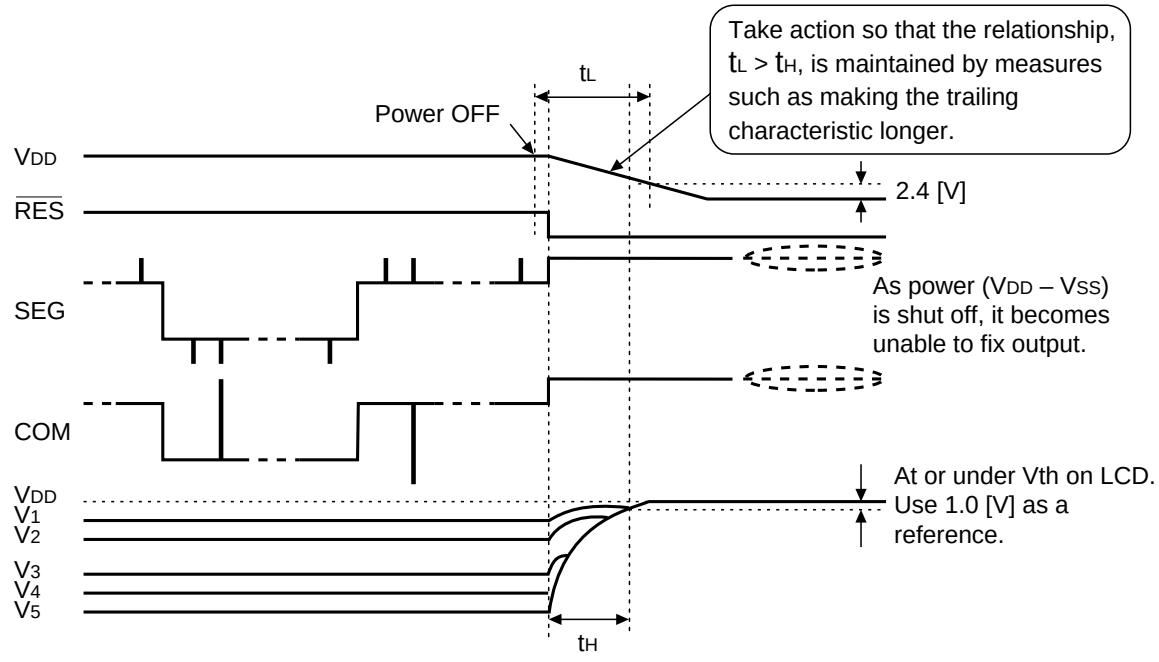


Fig. 21



If command control is disabled when power is OFF, take action so that the relationship, $t_L > t_H$, is maintained by measures such as making the trailing characteristic of power ($V_{DD} – V_{SS}$) longer.

Fig. 22

9. ABSOLUTE MAXIMUM RATINGS

Table 17

V_{SS}=0 V unless specified otherwise

Item		Symbol	Specification value			Unit
Power supply voltage		V_{DD}	–0.3	to	+7.0	V
Power supply voltage (2) (Based on V_{DD})		V_{SS2}	–7.0	to	+0.3	
	At triple boosting		–6.0	to	+0.3	
	At quadruple boosting		–4.5	to	+0.3	
Power supply voltage (3) (Based on V_{DD})		V_5, V_{OUT}	–20.0	to	+0.3	
Power supply voltage (4) (Based on V_{DD})		V_1, V_2, V_3, V_4	V_5	to	+0.3	
Input voltage		V_{IN}	–0.3	to	V_{DD}+0.3	
Output voltage		V_O	–0.3	to	V_{DD}+0.3	
Operating temperature		T_{OPR}	–40	to	+85	°C
Storage temperature	TCP	T_{STR}	–55	to	+100	
	Bare chip		–55	to	+125	

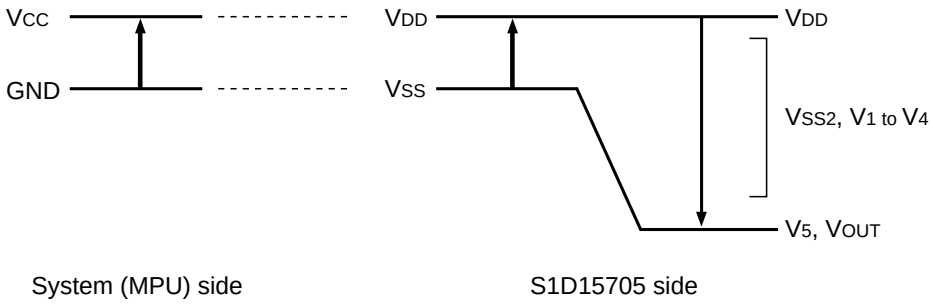


Fig. 23

(Notes) 1. The values of the V_{SS2}, V_1 to V_5, and V_{OUT} voltages are based on V_{DD}=0 V.
2. The V_1, V_2, V_3, and V_4 voltages must always satisfy the condition of $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$.
3. The V_{SS2} and V_{OUT} voltages must always satisfy the condition of $V_{DD} \geq V_{SS} \geq V_{SS2} \geq V_{OUT}$.
4. When LSI is used exceeding the absolute maximum ratings, the LSI may be damaged permanently. Besides, it is desirable that the LSI should be used in the electrical characteristics condition for normal operation. If this condition is exceeded, the LSI may malfunction and have an adverse effect on the reliability of the LSI.

10. DC CHARACTERISTICS

Table 18

Unless otherwise specified, V_{SS}=0 V, Ta=–40 to +85°C

Item	Symbol	Condition	Specification value Min.	Typ.	Max.	Unit	Applicable pin
Operating voltage (1)	V_{DD}	S1D15705⋆03⋆⋆/S1D15707⋆03⋆⋆	2.4	—	3.6	V	V_{DD} *1
	V_{DD}	S1D15705⋆00⋆⋆/S1D15707⋆00⋆⋆ /S1D15708⋆00⋆⋆	3.6	—	5.5		V_{DD} *1
Operating voltage (2)	V_{SS2}	(Based on VDD)	–6.0	—	–1.8		V_{SS2}
Operating voltage (3)	V_5	S1D15705⋆⋆⋆⋆⋆ (Based on V_{DD})	–18.0	—	–4.5		V_5 *2
	V_5	S1D15707⋆⋆⋆⋆⋆ (Based on V_{DD})	–16.0	—	–4.5		V_5 *2
	V_5	S1D15708⋆⋆⋆⋆⋆ (Based on V_{DD})	–10.0	—	–4.5		V_5 *2
	V_1, V_2	(Based on VDD)	0.4×V_5	—	V_{DD}		V_1, V_2
	V_3, V_4	(Based on V_{DD})	V_5	—	0.6×V_5		V_3, V_4
High level input voltage	V_{IHC}		0.8×V_{DD}	—	V_{DD}		*3
Low level input voltage	V_{ILC}		V_{SS}	—	0.2×V_{DD}		*3
High level output voltage	V_{OHC}	I_{OH}=–0.5mA	0.8×V_{DD}	—	V_{DD}		*4
Low level output voltage	V_{OLC}	I_{OL}=0.5mA	V_{SS}	—	0.2×V_{DD}		*4
Input leak current	I_{LI}	V_{IN}=V_{DD} or V_{SS}	–1.0	—	1.0	µA	*5
Output leak current	I_{LO}		–3.0	—	3.0		*6
Liquid crystal driver On resistance	R_{ON}	Ta=25°C, V_5=–14.0V	—	2.0	3.5	kΩ	SEGn
		(Based on V_{DD}) V_5=–8.0V	—	3.2	5.4		COMn *7
Static current consumption	I_{SSQ}		—	0.01	5	µA	V_{SS}, V_{SS2}
Output leak current	I_{5Q}	V_5=–18.0V (Based on V_{DD})	—	0.01	15		V_5
Input pin capacity	C_{IN}	Ta=25°C, f=1MHz	—	5.0	8.0	pF	
Oscillating frequency: Built-in oscillation	f_{OSC}	Ta=25°C	18	22	26		*8
Oscillating frequency: External input	f_{CL}	Ta=25°C, S1D15705⋆⋆⋆⋆⋆	4.5	5.5	6.5	kHz	CL *8
		Ta=25°C, S1D15707⋆⋆⋆⋆⋆	2.25	2.75	3.25		CL *8
		Ta=25°C, S1D15708⋆⋆⋆⋆⋆	1.13	1.38	1.63		CL *8

Table 19

Item		Symbol	Condition	Specification value Min.	Typ.	Max.	Unit	Applicable pin
Built-in power supply circuit	Input voltage	V_{SS2}	At triple boosting (Based on V_{DD})	–6.0	—	–1.8	V	V_{SS2}
		V_{SS2}	At quadruple boosting (Based on V_{DD})	–4.5	—	–1.8		V_{SS2}
	Boosting output voltage	V_{OUT}	(Based on V_{DD})	–20.0	—	—		V_{OUT}
	Voltage adjusting circuit operating voltage	V_{OUT}	(Based on V_{DD})	–20.0	—	–6.0		V_{OUT}
	V/F circuit operating voltage	V_5	S1D15705⋆⋆⋆⋆⋆ (Based on V_{DD})	–18.0	—	–4.5		V_5 *9
		V_5	S1D15707⋆⋆⋆⋆⋆ (Based on V_{DD})	–16.0	—	–4.5		V_5 *9
		V_5	S1D15708⋆⋆⋆⋆⋆ (Based on V_{DD})	–10.0	—	–4.5		V_5 *9
	Reference voltage	V_{REG0}	Ta=25°C, –0.05%/°C	–2.04	–2.10	–2.16		*10

[*: see Page 61.]

Dynamic current consumption value (1) During display operation and built-in power supply OFF
Current values dissipated by the whole IC when the external power supply is used

Table 20-1 Display All White Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15705⋆00⋆⋆	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	22	37	µA	*11
S1D15705⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	22	37		
S1D15707⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–8.0V		8	14		
S1D15707⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–8.0V		8	14		
S1D15708⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–6.0V		4	7		

Table 20-2 Display Checker Pattern Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
S1D15705⋆00⋆⋆	I_{DD} (1)	V_{DD}=5.0V, V_5–V_{DD}=–11.0V	—	33	55	µA	*11
S1D15705⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–11.0V	—	32	54		
S1D15707⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–8.0V		14	24		
S1D15707⋆03⋆⋆		V_{DD}=3.0V, V_5–V_{DD}=–8.0V		14	24		
S1D15708⋆00⋆⋆		V_{DD}=5.0V, V_5–V_{DD}=–6.0V		5	9		

Dynamic current consumption value (2) During display operation and built-in power supply ON
Current values dissipated by the whole IC containing the built-in power supply circuit

Table 21-1 Display Checker Pattern Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15705⋆00⋆⋆	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	73	122	µA	*12
		V_5–V_{DD}=–11.0V	High power mode	—	216	360		
S1D15705⋆03⋆⋆		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	92	154		
		V_5–V_{DD}=–11.0V	High power mode	—	272	454		
S1D15707⋆00⋆⋆		V_{DD}=5.0V, Triple boosting	Normal mode	—	40	67		
		V_5–V_{DD}=–8.0V	High power mode	—	171	285		
S1D15707⋆03⋆⋆		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	51	85		
		V_5–V_{DD}=–8.0V	High power mode	—	228	380		
S1D15708⋆00⋆⋆		V_{DD}=5.0V, Double boosting	Normal mode	—	28	47		
		V_5–V_{DD}=–6.0V	High power mode	—	137	229		

[*: see Page 61.]

Table 21-2 Display Checker Pattern Ta=25°C

Item	Symbol	Condition		Specification value			Unit	Remarks
				Min.	Typ.	Max.		
S1D15705∗00∗∗	I_{DD} (2)	V_{DD}=5.0V, Triple boosting	Normal mode	—	97	162	μA	*12
		V_5–V_{DD}=–11.0V	High power mode	—	254	424		
S1D15705∗03∗∗		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	130	217		
		V_5–V_{DD}=–11.0V	High power mode	—	308	514		
S1D15707∗00∗∗		V_{DD}=5.0V, Triple boosting	Normal mode	—	54	90		
		V_5–V_{DD}=–8.0V	High power mode	—	185	309		
S1D15707∗03∗∗		V_{DD}=3.0V, Quadruple boosting	Normal mode	—	71	119		
		V_5–V_{DD}=–8.0V	High power mode	—	248	414		
S1D15708∗00∗∗		V_{DD}=3.0V, Double boosting	Normal mode	—	35	59		
		V_5–V_{DD}=–6.0V	High power mode	—	144	240		

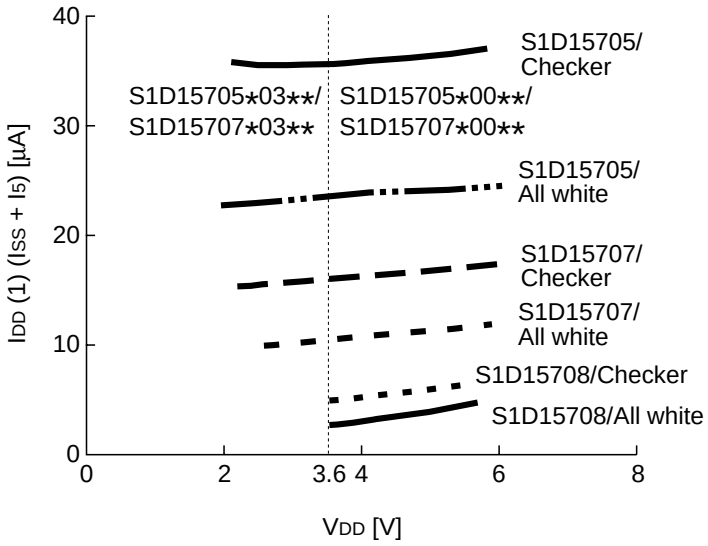
Current consumption at power save V_{SS}=0 V and V_{DD}= 3.0 V ±10% (S1D15705∗03∗∗, S1D15707∗03∗∗)
5.0V ± 10% (S1D15705∗00∗∗, S1D15707∗00∗∗, S1D15708∗00∗∗)

Table 22 Ta=25°C

Item	Symbol	Condition	Specification value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}	Ta=25°C	—	0.01	5	μA	
Stand-by state	I_{DDS2}	Ta=25°C	—	4	8		

[*: see Page 61.]

[Reference data 1]
• Dynamic current consumption (1) External power supply used and LCD being displayed

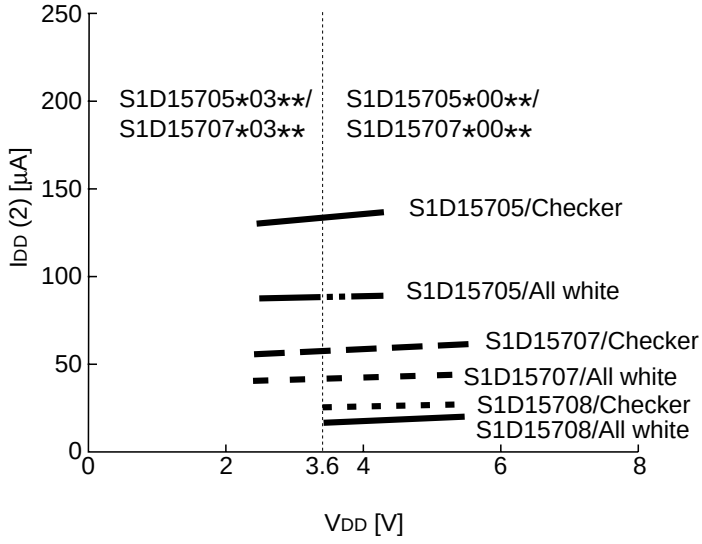


Condition: Built-in power supply OFF
External power supply used
S1D15705: $V_5 - V_{DD} = -11.0$ V
S1D15707: $V_5 - V_{DD} = -8.0$ V
S1D15708: $V_5 - V_{DD} = -6.0$ V
Display pattern: All white/checker
Ta = 25°C

Remarks: *11

Fig. 24

[Reference data 2]
• Dynamic current consumption (2) Built-in power supply used and LCD being displayed



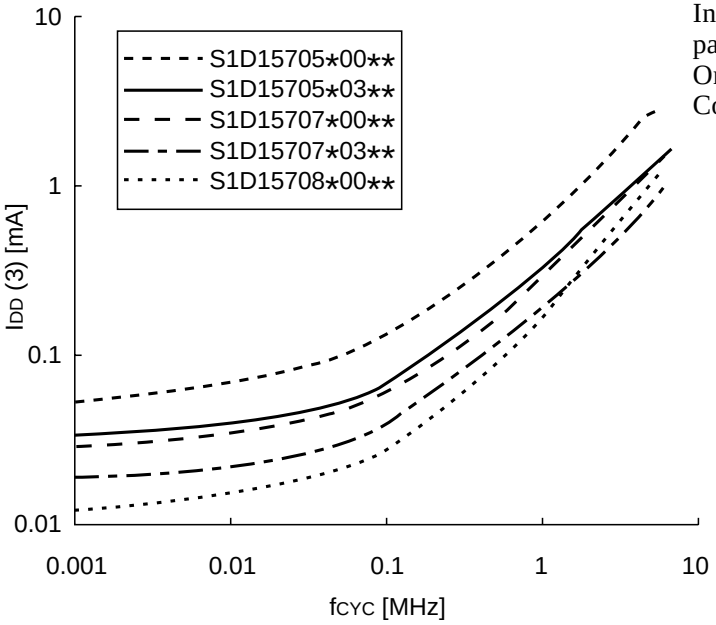
Condition: Built-in power supply ON
Normal mode
Quadruple boosting
S1D15705: $V_5 - V_{DD} = -11.0$ V
Triple boosting
S1D15707: $V_5 - V_{DD} = -8.0$ V
Double boosting
S1D15708: $V_5 - V_{DD} = -6.0$ V
Display pattern: All white/checker
Ta = 25°C

Remarks: *12

Fig. 25

[*: see page 61.]

[Reference data 3]
• Dynamic current consumption (3) During access



Indicates the current consumption when the checker pattern is always written at f_{CYC}.
Only I_{DD} (1) when not accessed
Condition: Built-in power supply OFF and external power supply used
S1D15705:
$V_5 - V_{DD} = -11.0$ V
S1D15707:
$V_5 - V_{DD} = -11.0$ V
S1D15705∗03∗∗/S1D15707∗03∗∗:
$V_{DD} - V_{SS} = 3.0$ V
S1D15705∗00∗∗/S1D15707∗00∗∗
/S1D15708∗00∗∗:
$V_{DD} - V_{SS} = 5.0$ V
Ta = 25°C

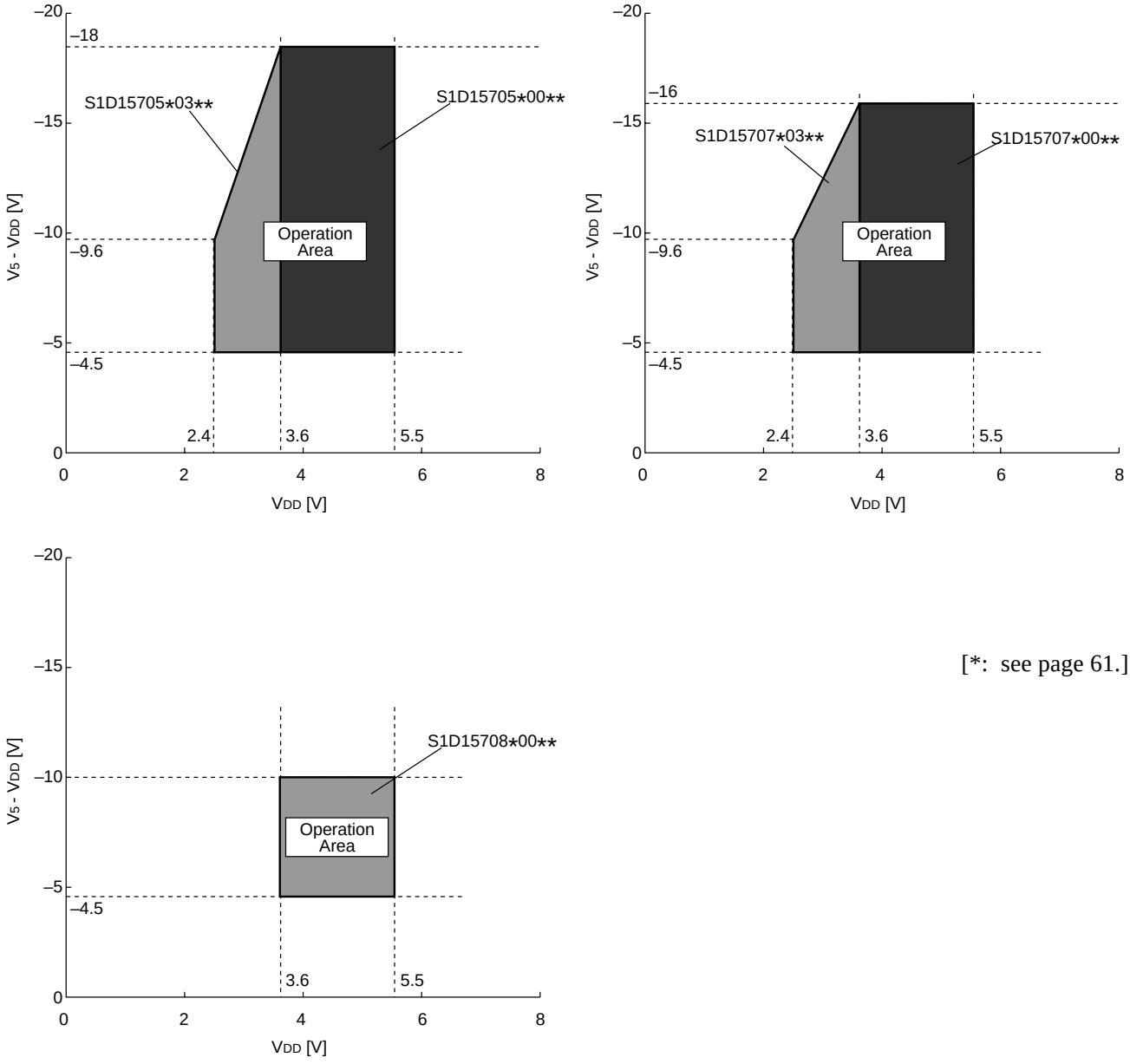
[*: see page 61.]

Fig. 26

[Reference data 4]

VSS and V5 system operating voltage ranges

Remarks: *2



[*: see page 61.]

Fig. 27

Relationships between the oscillating frequency fOSC, display clock frequency fCL, and liquid crystal frame frequency fFR

Table 23

Item		fCL	fFR	
			Normal duty drive	n-line reverse drive
S1D15705*****	When built-in oscillator circuit used	$\frac{f_{OSC}}{4}$	$\frac{f_{OSC}}{4.65}$	$\frac{f_{OSC}}{4.n}$
	When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{65}$	$\frac{f_{CL}}{n}$
S1D15707*****	When built-in oscillator circuit used	$\frac{f_{OSC}}{8}$	$\frac{f_{OSC}}{8.33}$	$\frac{f_{OSC}}{8.n}$
	When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{33}$	$\frac{f_{CL}}{n}$
S1D15708*****	When built-in oscillator circuit used	$\frac{f_{OSC}}{16}$	$\frac{f_{OSC}}{16.17}$	$\frac{f_{OSC}}{16.n}$
	When built-in oscillator circuit not used	External input (fCL)	$\frac{f_{CL}}{17}$	$\frac{f_{CL}}{n}$

(fFR shows the alternating current cycle (frame cycle) of liquid crystal. The signal of FR terminal becomes twice as a frame cycle.)

[Reference items marked by *]

*1 The wide operating voltage range is not warranted. However, when there is a sudden voltage change during MPU access, it cannot be warranted.

*2 For the VDD and V5 operating voltage ranges, see Fig. 27. These ranges are applied when using the external power supply.

*3 A0, D0 to D5, D6 (SCL), D7 (SI), $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$, $\overline{IRS}$ and $\overline{HPM}$ pins

*4 D0 to D7, FR, FRS, $\overline{DOF}$ and CL pins

*5 A0, $\overline{RD}$ (E), $\overline{WR}$ (R/W), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$, IRS and $\overline{HPM}$ pins

*6 Applied when D0 to D5, D6 (SCL), D7 (SI), CL, FR, and $\overline{DOF}$ pins are in the high impedance state

*7 Resistance value when the 0.1 V voltage is applied between the output pin SEGn or COMn and power supply pins (V1, V2, V3, and V4). Specified within the range of operating voltage (3)
RON = 0.1 V/ΔI (ΔI indicates the current applied when 0.1 V is applied between the power ON.)

*8 For the relationship between the oscillating frequency and frame frequency, see Table 23. The specification value of the external input item is a recommended value.

*9 The V5 voltage adjusting circuit is adjusted within the voltage follower operating voltage range.

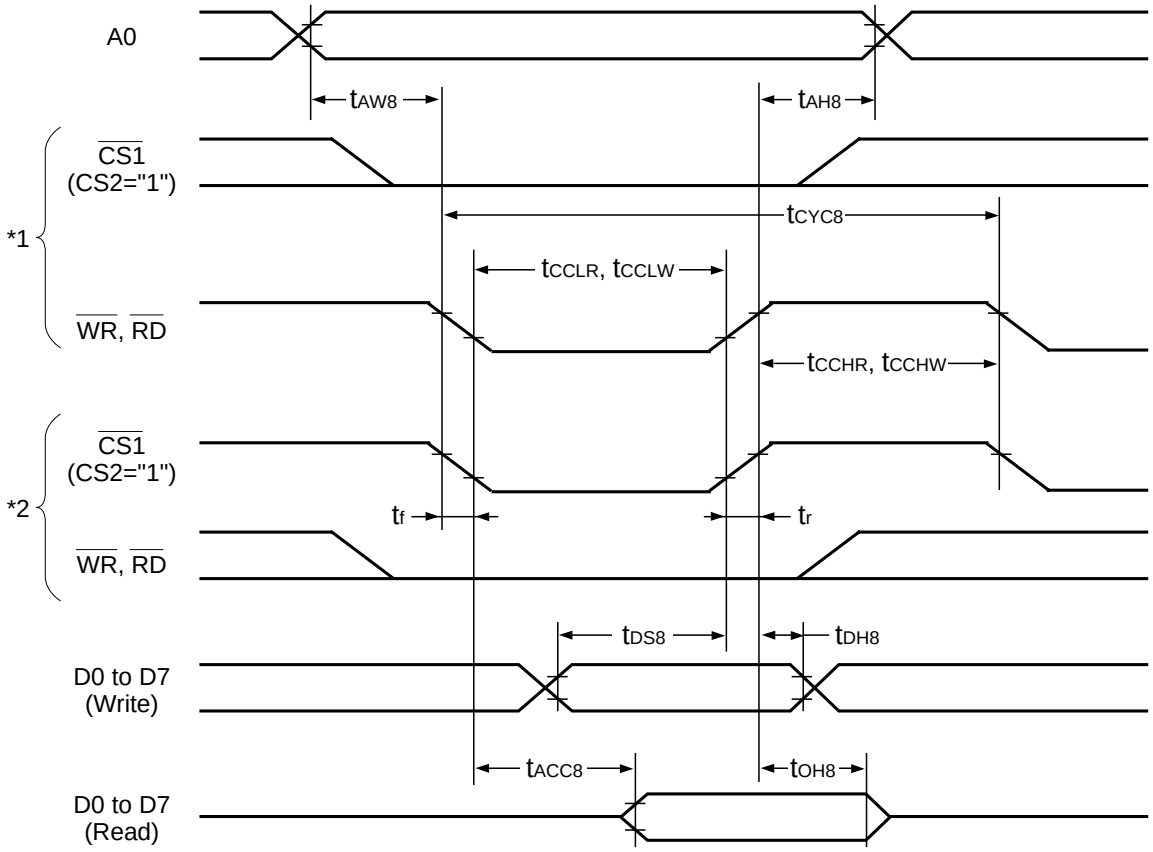
*10 Built-in reference voltage source of the V5 voltage adjusting circuit.

*11 and *12 Indicate the current dissipated by a single IC at built-in oscillator circuit used, 1/9 bias (S1D15705*****), 1/6 bias (S1D15707*****/S1D15708*****), and display ON. Does not include the current due to the LCD panel capacity and wireing capacity. Applicable only when there is no access from the MPU.

*12 When the V5 voltage adjusting built-in resistor is used

Timing Characteristics

System bus read/write characteristics 1 (80 series MPU)



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		250	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		30	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		70	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		30	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		30	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	70	
Output disable time		t_{OH8}		5	50	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to +85°C]

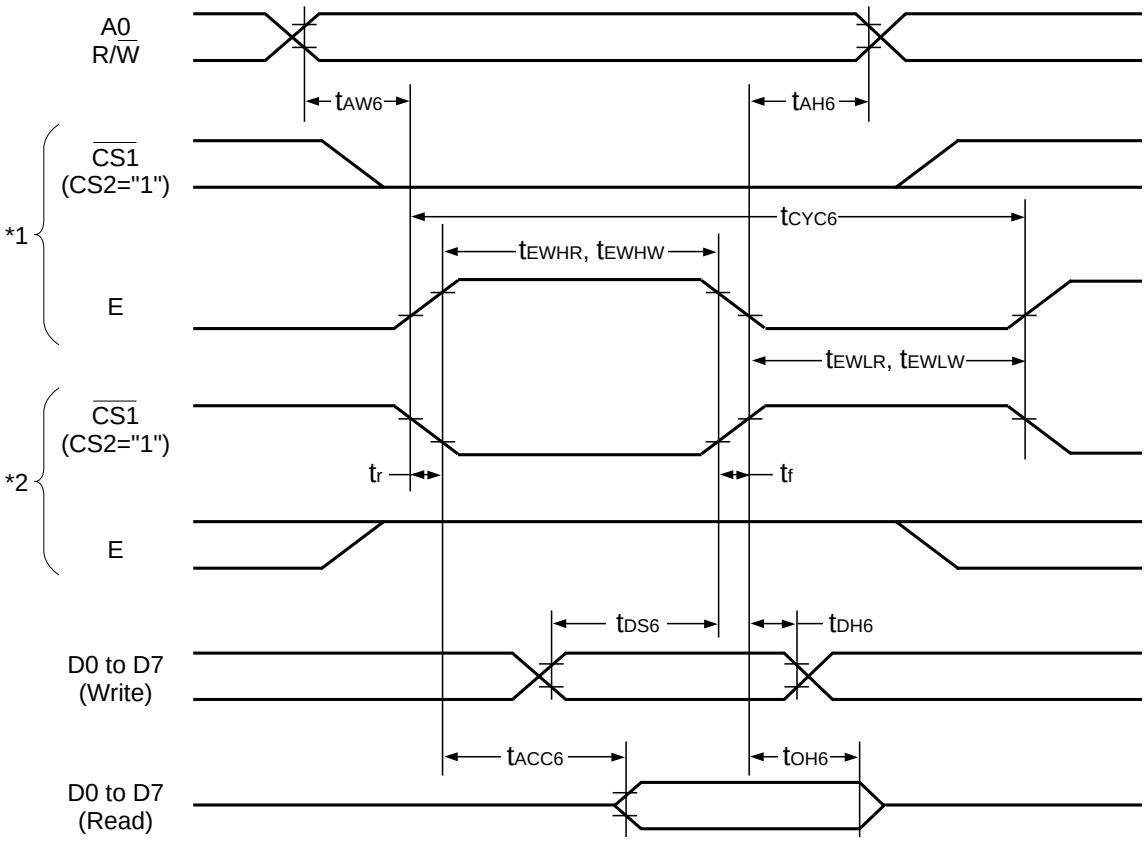
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		300	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		60	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		120	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		60	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		60	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		15	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	280	
Output disable time		t_{OH8}		10	100	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to3.6V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		800	—	
Control LOW pulse width (Write)	$\overline{WR}$	t_{CCLW}		120	—	
Control LOW pulse width (Read)	$\overline{RD}$	t_{CCLR}		240	—	
Control HIGH pulse width (Write)	$\overline{WR}$	t_{CCHW}		120	—	
Control HIGH pulse width (Read)	$\overline{RD}$	t_{CCHR}		120	—	
Data setup time	D0 to D7	t_{DS8}		80	—	
Data hold time		t_{DH8}		30	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	280	
Output disable time		t_{OH8}		10	200	

*1 This is in the case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS1}$=LOW.
*2 This is in the case of making the access by $\overline{CS1}$, setting the $\overline{WR}$, $\overline{RD}$=LOW.
*3 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for (t_r+t_f) ≤ (t_{CYC8}–t_{CCLW}–t_{CCHW}) or (t_r+t_f) ≤ (t_{CYC8}–t_{CCLR}–t_{CCHR}).
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{CCLW} and t_{CCLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2= HIGH) level and $\overline{WR}$, $\overline{RD}$ are at the LOW level.

System bus read/write characteristics 2 (68 series MPU)



[S1D15705∗00∗∗, S1D15707∗00∗∗, S1D15708∗00∗∗: V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		250	—	
Data setup time		D0 to D7	t_{DS6}		30	—	
Data hold time			t_{DH6}		10	—	
Access time			t_{ACC6}	C_L=100pF	—	70	
Output disable time			t_{OH6}		5	50	
Enable HIGH pulse width	Read	E	t_{EWHR}		70	—	
	Write		t_{EWHW}		30	—	
Enable LOW pulse width	Read	E	t_{EWLR}		30	—	
	Write		t_{EWLW}		30	—	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to +85°C]

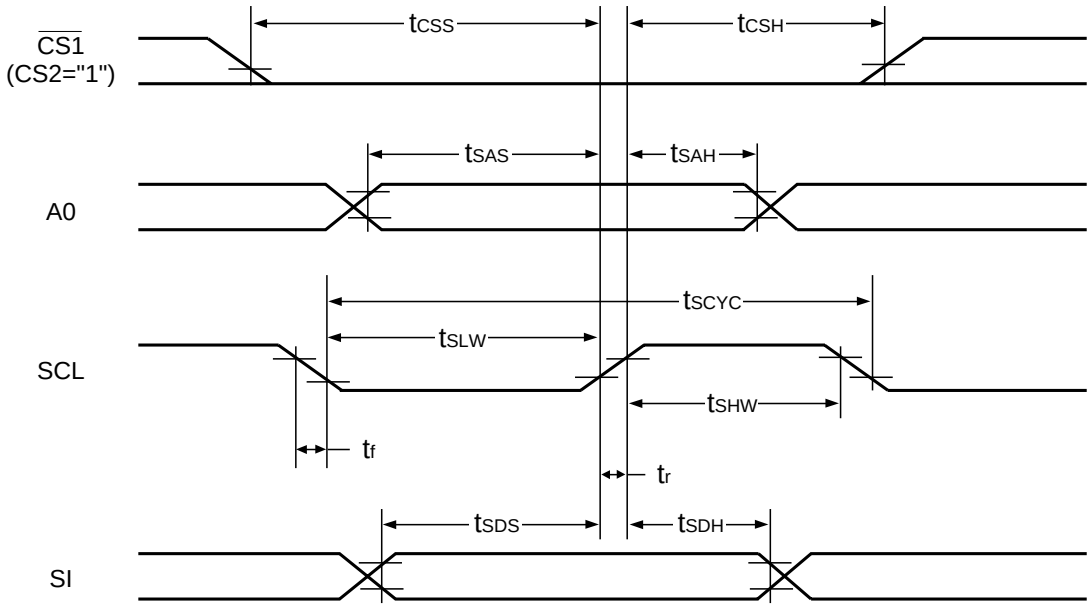
Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		300	—	
Data setup time		D0 to D7	t_{DS6}		40	—	
Data hold time			t_{DH6}		15	—	
Access time			t_{ACC6}	C_L=100pF	—	140	
Output disable time			t_{OH6}		10	100	
Enable HIGH pulse width	Read	E	t_{EWHR}		120	—	
	Write		t_{EWHW}		60	—	
Enable LOW pulse width	Read	E	t_{EWLR}		60	—	
	Write		t_{EWLW}		60	—	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to +85°C]

Item		Signal	Symbol	Condition	Specification value		Unit
					Min.	Max.	
Address hold time		A0	t_{AH6}		0	—	ns
Address setup time			t_{AW6}		0	—	
System cycle time			t_{CYC6}		800	—	
Data setup time		D0 to D7	t_{DS6}		80	—	
Data hold time			t_{DH6}		30	—	
Access time			t_{ACC6}	C_L=100pF	—	280	
Output disable time			t_{OH6}		10	200	
Enable HIGH pulse width	Read	E	t_{EWHR}		240	—	
	Write		t_{EWHW}		120	—	
Enable LOW pulse width	Read	E	t_{EWLR}		120	—	
	Write		t_{EWLW}		120	—	

*1 This is in the case of making the access by E, setting the $\overline{CS1}$=LOW.
*2 This is in the case of making the access by $\overline{CS1}$, setting the E=HIGH.
*3 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns. When using the system cycle time at high speed, they are specified for $(t_r+t_f) \leq (t_{CYC6}–t_{EWLW}–t_{EWHW})$ or $(t_r+t_f) \leq (t_{CYC6}–t_{EWLR}–t_{EWHR})$.
*4 All timings are specified based on the 20 and 80% of V_{DD}.
*5 t_{EWLW} and t_{EWLR} are specified for the overlap period when $\overline{CS1}$ is at LOW (CS2= HIGH) level and E is at the HIGH level.

Serial interface



[S1D15705∗00∗∗, S1D15707∗00∗∗, S1D15708∗00∗∗: V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		200	—	ns
SCL HIGH pulse width		t_{SHW}		75	—	
SCL LOW pulse width		t_{SLW}		75	—	
Address setup time	A0	t_{SAS}		50	—	
Address hold time		t_{SAH}		100	—	
Data setup time	SI	t_{SDS}		50	—	
Data hold time		t_{SDH}		50	—	
CS-SCL time	CS	t_{CSS}		100	—	
		t_{CSH}		100	—	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to +85°C]

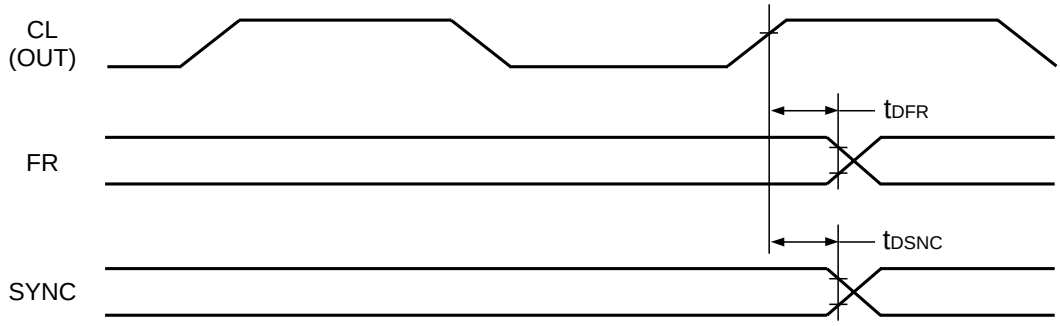
Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		250	—	ns
SCL HIGH pulse width		t_{SHW}		100	—	
SCL LOW pulse width		t_{SLW}		100	—	
Address setup time	A0	t_{SAS}		150	—	
Address hold time		t_{SAH}		150	—	
Data setup time	SI	t_{SDS}		100	—	
Data hold time		t_{SDH}		100	—	
CS-SCL time	CS	t_{CSS}		150	—	
		t_{CSH}		150	—	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value		Unit
				Min.	Max.	
Serial clock cycle	SCL	t_{SCYC}		400	—	ns
SCL HIGH pulse width		t_{SHW}		150	—	
SCL LOW pulse width		t_{SLW}		150	—	
Address setup time	A0	t_{SAS}		250	—	
Address hold time		t_{SAH}		250	—	
Data setup time	SI	t_{SDS}		150	—	
Data hold time		t_{SDH}		150	—	
CS-SCL time	CS	t_{CSS}		250	—	
		t_{CSH}		250	—	

*1 The rise and fall times (tr and tf) of the input signal are specified for less than 15 ns.
*2 All timings are specified based on the 20 and 80% of V_{DD}.

Display control output timing



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	10	40	ns
SYNC delay time	SYNC	t_{DSNC}	C_L=50pF	—	10	40	ns

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to +85°C]

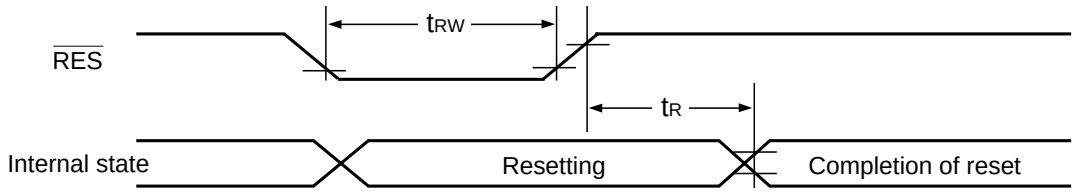
Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	20	80	ns
SYNC delay time	SYNC	t_{DSNC}	C_L=50pF	—	20	80	ns

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L=50pF	—	50	200	ns
SYNC delay time	SYNC	t_{DSNC}	C_L=50pF	—	50	200	ns

*1 Valid only when the master mode is selected.
*2 All timings are specified based on the 20 and 80% of V_{DD}.
*3 Pay attention not to cause delays of the timing signals CL, FR and SYNC to the salve side by wiring resistance, etc., while master/slave operations are in progress. If these delays occur, indication failures such as flickering may occur.

Reset input timing



[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=4.5V to 5.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	0.5	µs
Reset LOW pulse width	RES	t_{RW}		0.5	—	—	

[S1D15705⋆00⋆⋆, S1D15707⋆00⋆⋆, S1D15708⋆00⋆⋆: V_{DD}=3.6V to 4.5V, Ta=–40 to +85°C]

Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1	µs
Reset LOW pulse width	RES	t_{RW}		1	—	—	

[S1D15705⋆03⋆⋆, S1D15707⋆03⋆⋆: V_{DD}=2.4V to 3.6V, Ta=–40 to +85°C]

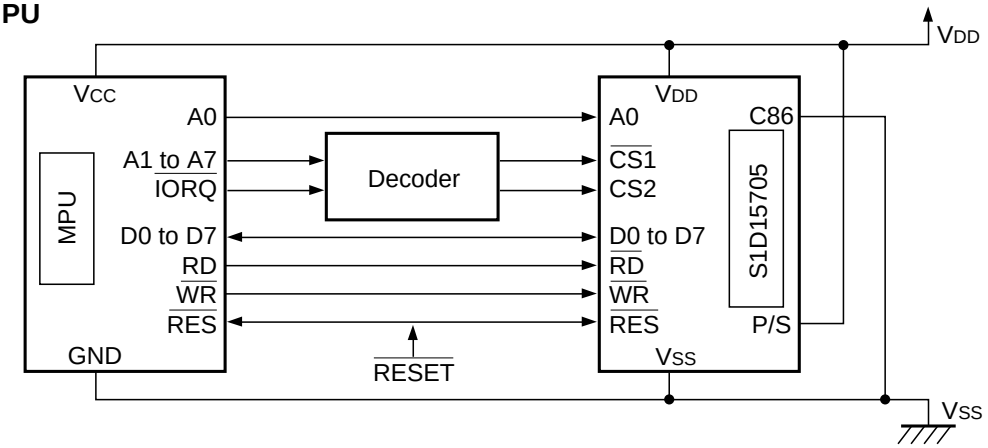
Item	Signal	Symbol	Condition	Specification value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset LOW pulse width	RES	t_{RW}		1.5	—	—	

*1 All timings are specified based on the 20 and 80% of V_{DD}.

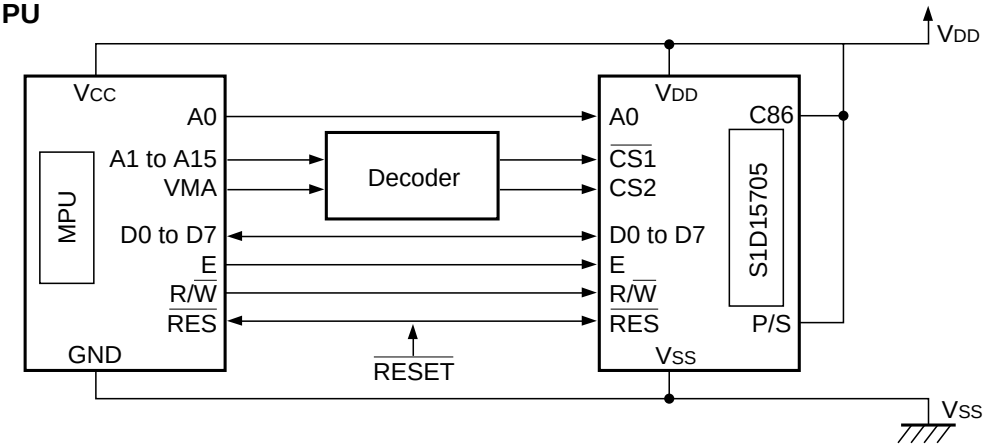
11. MICROPROCESSOR (MPU) INTERFACE: REFERENCE

The S1D15705 series can directly be connected to the 80 system MPU and 68 series MUP. It can also be operated with a fewer signal lines by using the serial interface.
The S1D15705 series is used for the multiple chip configuration to expand the display area. In this case, it can select the ICs that are accessed individually using the Chip Select signal.
After the initialization using the $\overline{RES}$ pin, the respective input pins of the S1D15705 series need to be controlled normally.

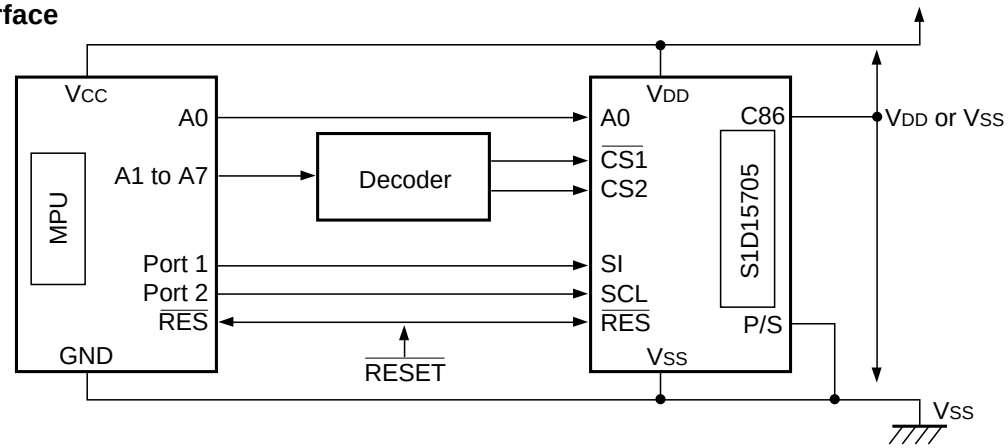
80 series MPU



68 series MPU



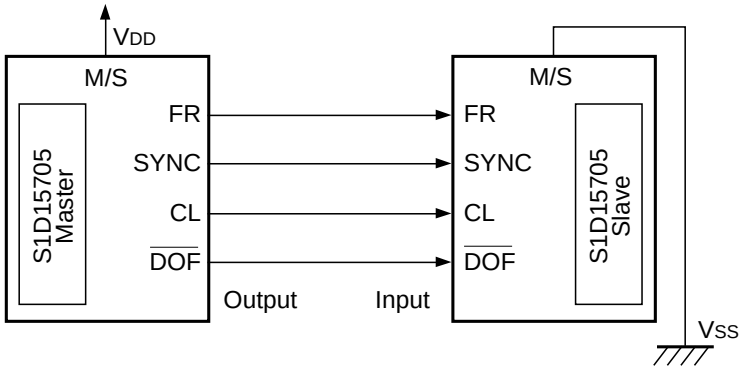
Serial interface



12. CONNECTION BETWEEN LCD DRIVERS: REFERENCE

The S1D15705 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15705*****/S1D15705*****, S1D15707*****/S1D15707***** or S1D15708*****/S1D15708*****) for the master/slave.

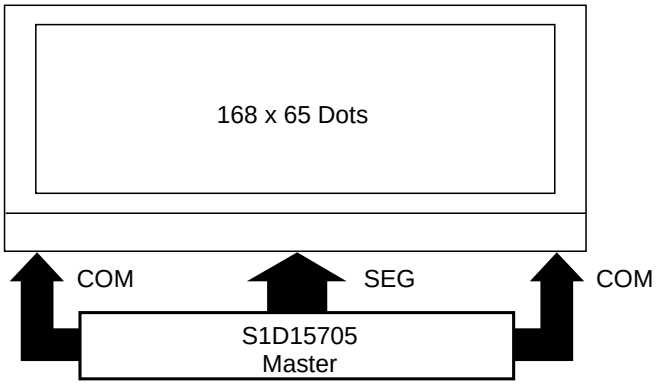
S1D15705 (master) ↔ S1D15705 (slave)



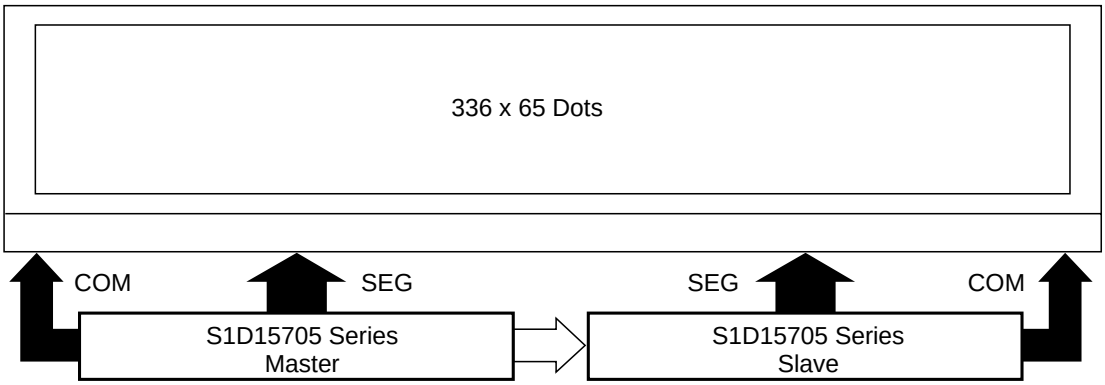
13. LCD PANEL WIRING: REFERENCE

The S1D15705 series is used for the multiple chip configuration to easily expand the liquid crystal display area. Use the same device (S1D15705*****/S1D15705*****, S1D15707*****/S1D15707***** or S1D15708*****/ S1D15708*****) for the multiple chip configuration.

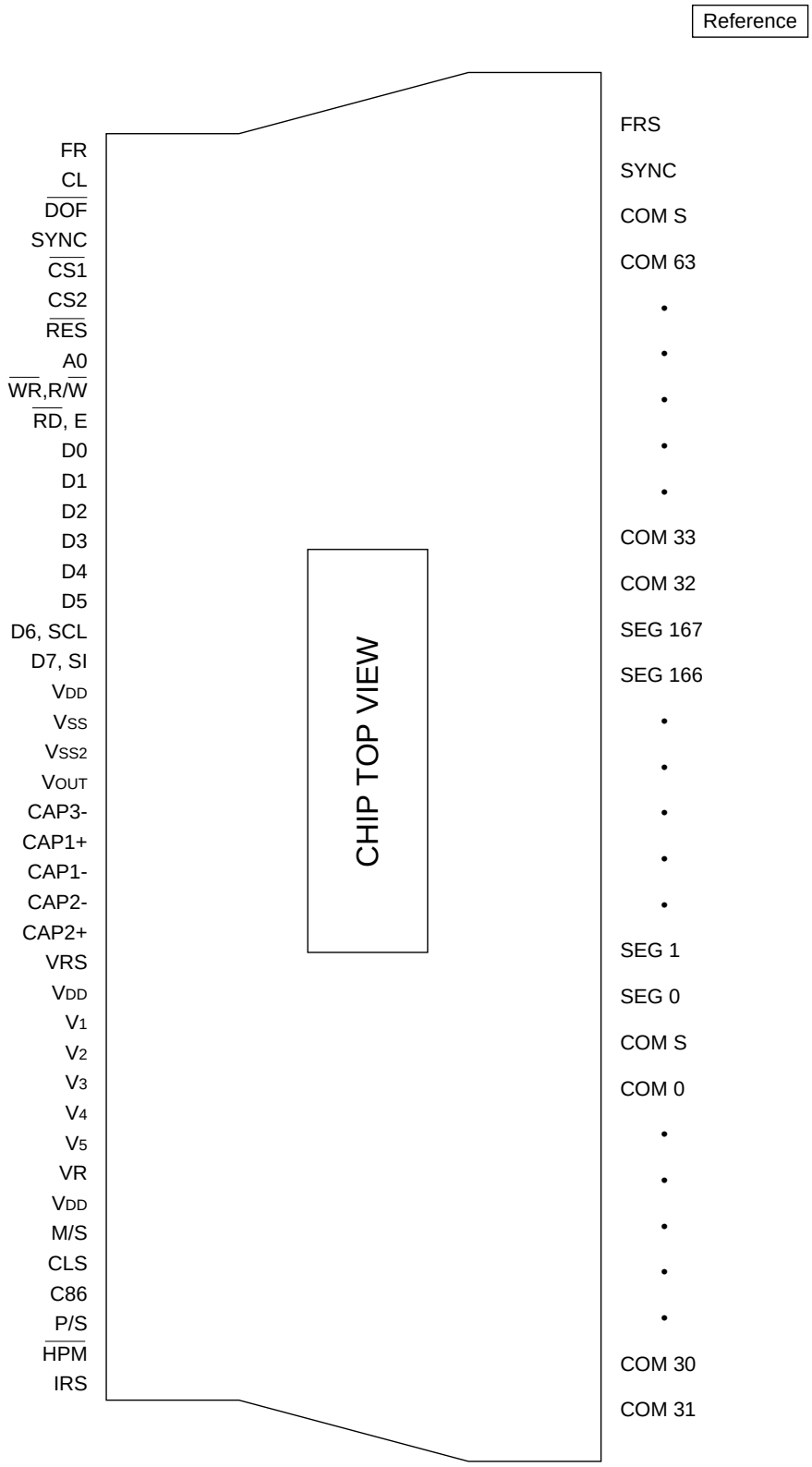
1-chip configuration



2-chip configuration

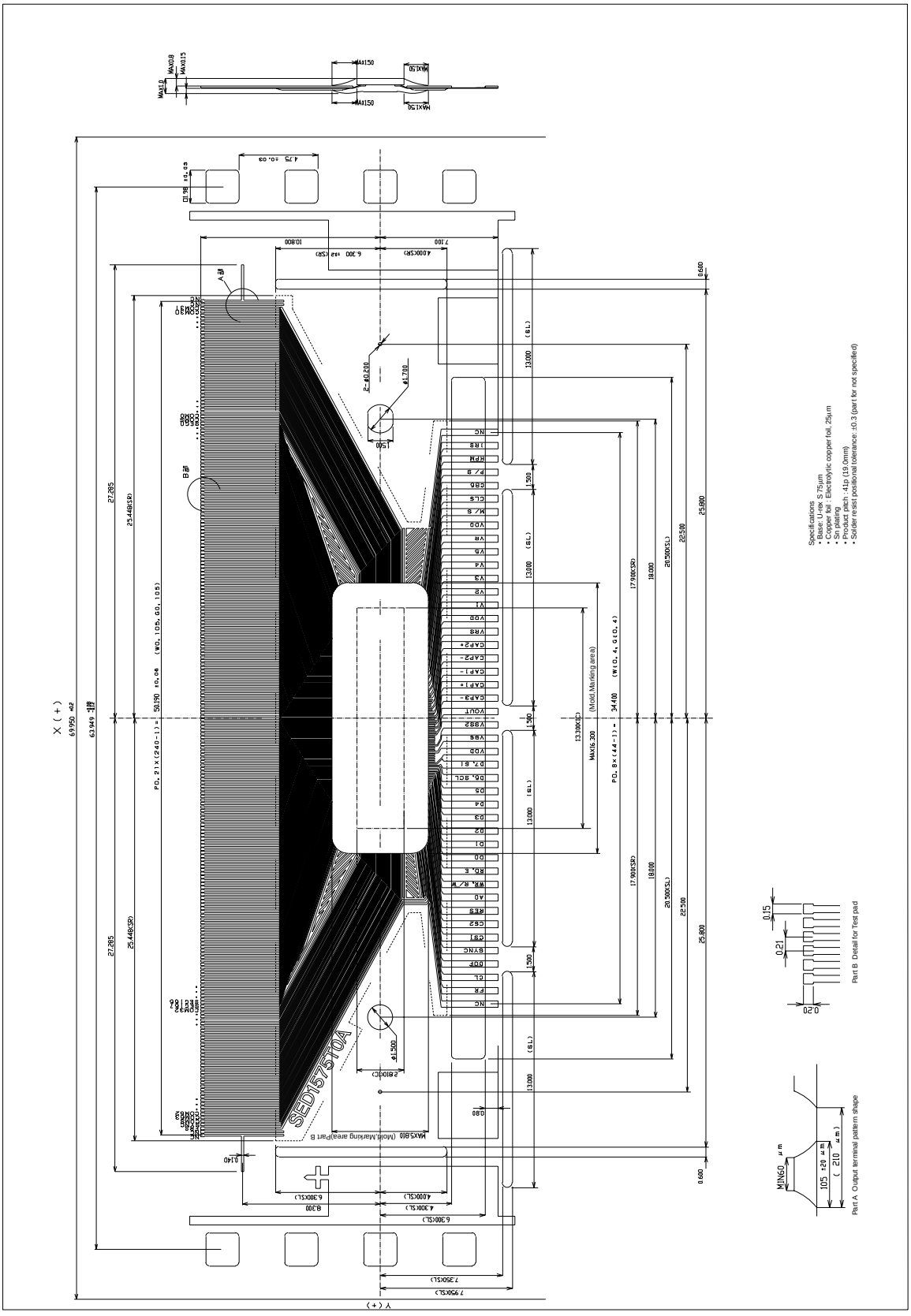


14. TCP PIN LAYOUT



Note) This TCP pin layout does not specify the TCP dimensions.

15. TCP DIMENSIONS



16. TEMPERATURE SENSOR CIRCUIT

S1D15705∗10∗∗ incorporates a temperatujre sensor circuit with a 11.4mV/°C (typ.) temperature gradient carrying analog voltage output pins. The S1D15705∗10∗∗ makes it possible to provide LCD indications with optimum contrast throughout a wide temperature range without need for use of supplementary parts by inputting electronic volume control registration value equivalent signals corresponding to the outputs of the temperature sensor through the MPU to control the LCD drive voltage V_5.
For LCD drive voltage controls of higher precision, we recommend you to constitute a system which can absorb deviations of the output voltage by, such as, feeding back sampled output voltages under a certain temperature environment to the MPU to let it memorize as the reference voltages.
Regarding the specifications of other items than the temperature sensor circuit, such as of the absolute maximum ratings, DC characteristics, AC characteristics, etc., refer to the specifications for S1D15705∗00∗∗.

Pin Definitions

Temperature sensor circuit related pins are allocated to TEST1, 2, 3 and 4 and the pin names are TEST1, SVS, V_{SEN}, SEN and SENSEL in the given sequence. The temperature sensor should be used under the pin statuses indicated in the Table below. When the temperature sensor is not being used, fix respective pins to HIGH.

Pin names	I/O	Pin definitions	Number of pins
SVS	Power supply	This is the power supply pin for the temperature sensor. Apply prescribed operating voltage between the V_{DD}.	1
V_{SEN}	O	This is the analog voltage output pin for the temperature sensor. Monitor the output voltage between the V_{DD}.	1
SEN	O	Consider to keep this pin open in order not to apply the load capacitance of wires, etc.	1
SENSEL	I	Fix this pin to HIGH.	1

Electric Characteristics

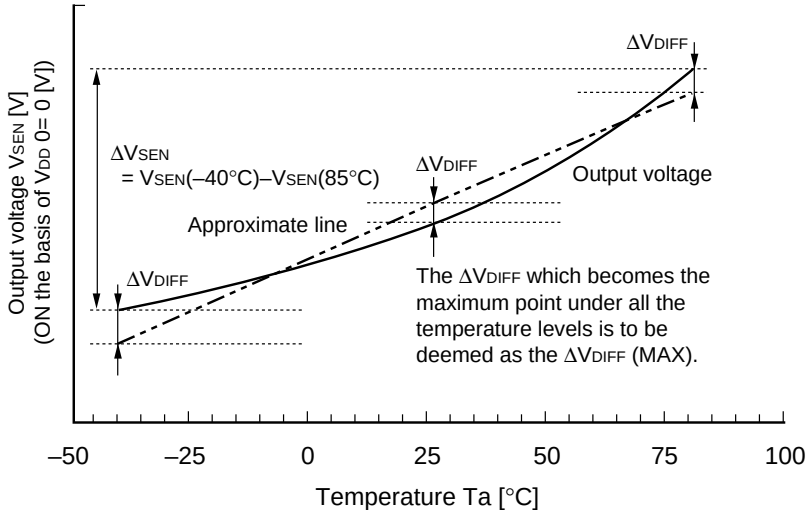
Items	Codes	Conditions	Specifications			Units	Applicable pins
			Min.	Typ.	Max.		
Operating voltage	SVS	(On the basis of V_{DD})	–5.5	–5.0	–4.5	V	SVS
Output voltage	V_{SEN}	(On the basis of V_{DD}) Ta = 40°C	–4.35	–3.62	–2.89	V	V_{SEN}
		(On the basis of V_{DD}) Ta = 25°C	–3.48	–2.88	–2.28		
		(On the basis of V_{DD}) Ta = 85°C	–2.92	–2.20	–1.47		
Output voltage temperature gradient	V_{GRA}	*1	9.4	11.4	13.4	mV/°C	V_{SEN}
Output voltage linearity	ΔV_L	*2	–1.5	—	1.5	%	V_{SEN}
Output voltage setup time	t_{SEN}	*3	100	—	—	mS	V_{SEN}
Operating current	I_{SEN}	Ta = 25°C	—	40	150	µA	SVS

[* Notes]

*1: Represents the gradient of the approximate line of the Typ. output voltages.

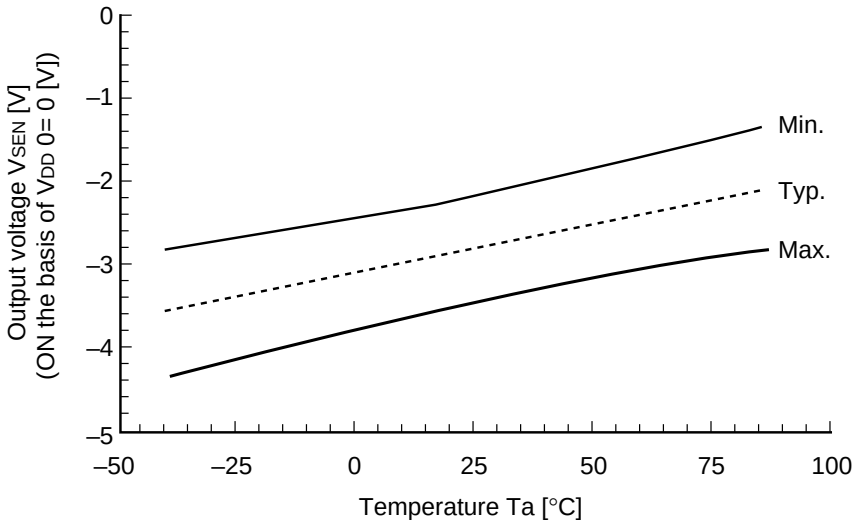
*2: Represents the maximum deviation between the output voltage curve and the approximate line. Assuming that the difference of output voltages at –40°C and at 80°C as ΔV_{SEN}, assuming that the difference between the approximate line and the output voltage values as ΔDIFF and assuming that the maximum value thereof as ΔDIFF (MAX), the output voltages linearity ΔV_L can be calculated by use of the following equation.

$$\Delta V_L = \frac{\Delta DIFF\ (MAX)}{\Delta V_{SEN}} \times 100$$



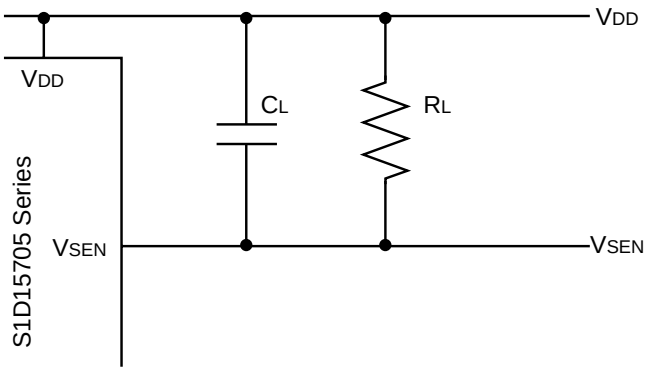
*3: Represents the queuing time after the supply voltage SVS is applied to the SVS pin until the output voltage is stabilized and monitoring thereof becomes feasible. Be sure to sample the output voltage after the prescribed queuing time has elapsed.

Output voltage characteristics



Output Pin Load

Maintain the load capacity C_L for the V_{SEN} output pin V_{SEN} at 100pF or less and keep the load resistance R_L for the V_{SEN} output pin V_{SEN} at 1MΩ or more.
In order to obtain accurate output voltage values, be careful not to insert a current flowing channel between the V_{SS}.



17. CAUTIONS

Cautions must be exercised on the following points when using this Development Specification:

1. This Development Specification is subject to change for engineering improvement.
2. This Development Specification does not guarantee execution of the industrial proprietary rights or other rights, or grant a license. Examples of applications described in This Development Specification are intended for your understanding of the Product. We are not responsible for any circuit problem or the like arising from the use of them.
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For the use of the semi-conductor,cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

(1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
(2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
(3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC

EPSON

International Sales Operations

AMERICA

EPSON ELECTRONICS AMERICA, INC.
HEADQUARTERS
150 River Oaks Parkway
San Jose, CA 95134, U.S.A.
Phone: +1-800-228-3964 FAX: +1-408-922-0238

SALES OFFICES

West
1960 E.Grand Avenue Flr 2
El Segundo, CA 90245, U.S.A.
Phone: +1-800-249-7730 FAX: +1-310-955-5400

Central
101 Virginia Street, Suite 290
Crystal Lake, IL 60014, U.S.A.
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Northeast
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Wakefield, MA 01880, U.S.A.
Phone: +1-800-922-7667 FAX: +1-781-246-5443

Southeast
3010 Royal Blvd. South, Suite 170
Alpharetta, GA 30005, U.S.A.
Phone: +1-877-332-0020 FAX: +1-770-777-2637

EUROPE

EPSON EUROPE ELECTRONICS GmbH
HEADQUARTERS
Riesstrasse 15
80992 Munich, GERMANY
Phone: +49-89-14005-0 FAX: +49-89-14005-110

DÜSSELDORF BRANCH OFFICE
Altstadtstrasse 176
51379 Leverkusen, GERMANY
Phone: +49-2171-5045-0 FAX: +49-2171-5045-10

FRENCH BRANCH OFFICE
1 Avenue de l' Atlantique, LP 915 Les Conquerants
Z.A. de Courtaboeuf 2, F-91976 Les Ulis Cedex, FRANCE
Phone: +33-1-64862350 FAX: +33-1-64862355

BARCELONA BRANCH OFFICE
Barcelona Design Center
Edificio Testa, C/Alcalde Barnils 64-68, Modulo C 2a planta
E-08190 Sant Cugat del Vallès, SPAIN
Phone: +34-93-544-2490 FAX: +34-93-544-2491

UK & IRELAND BRANCH OFFICE
8 The Square, Stockley Park, Uxbridge
Middx UB11 1FW, UNITED KINGDOM
Phone: +44-1295-750-216/+44-1342-824451
FAX: +44-89-14005 446/447

Scotland Design Center
Integration House, The Alba Campus
Livingston West Lothian, EH54 7EG, SCOTLAND
Phone: +44-1506-605040 FAX: +44-1506-605041

ASIA

EPSON (CHINA) CO., LTD.
23F, Beijing Silver Tower 2# North RD DongSanHuan
ChaoYang District, Beijing, CHINA
Phone: +86-10-6410-6655 FAX: +86-10-6410-7320

SHANGHAI BRANCH
7F, High-Tech Bldg., 900, Yishan Road,
Shanghai 200233, CHINA
Phone: +86-21-5423-5522 FAX: +86-21-5423-5512

EPSON HONG KONG LTD.
20/F., Harbour Centre, 25 Harbour Road
Wanchai, Hong Kong
Phone: +852-2585-4600 FAX: +852-2827-4346
Telex: 65542 EPSCO HX

EPSON Electronic Technology Development (Shenzhen) LTD.
12/F, Dawning Mansion, Keji South 12th Road,
Hi- Tech Park, Shenzhen
Phone: +86-755-2699-3828 FAX: +86-755-2699-3838

EPSON TAIWAN TECHNOLOGY & TRADING LTD.
14F, No. 7, Song Ren Road,
Taipei 110
Phone: +886-2-8786-6688 FAX: +886-2-8786-6677

HSINCHU OFFICE
No. 99, Jiangong Road,
Hsinchu City 300
Phone: +886-3-573-9900 FAX: +886-3-573-9169

EPSON SINGAPORE PTE., LTD.
1 HarbourFront Place,
#03-02 HarbourFront Tower One, Singapore 098633
Phone: +65-6586-5500 FAX: +65-6271-3182

SEIKO EPSON CORPORATION
KOREA OFFICE
50F, KLI 63 Bldg., 60 Yoido-dong
Youngdeungpo-Ku, Seoul, 150-763, KOREA
Phone: +82-2-784-6027 FAX: +82-2-767-3677

GUMI OFFICE
2F, Grand B/D, 457-4 Songjeong-dong,
Gumi-City, KOREA
Phone: +82-54-454-6027 FAX: +82-54-454-6093

SEIKO EPSON CORPORATION
SEMICONDUCTOR OPERATIONS DIVISION

IC Sales Dept.
IC Marketing Group
421-8, Hino, Hino-shi, Tokyo 191-8501, JAPAN
Phone: +81-42-587-5814 FAX: +81-42-587-5117

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