



TOPWAY displays

info@topwaydisplays.eu
www.topwaydisplays.eu

LMT057DNAFWU-AAN

LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Date:	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary New release	2007-04-13
0.2	Typing Correction in Dot Pitch	2007-04-20
0.3	Typing Correction in 6.3.3 Opcode [82] discription	2007-05-17
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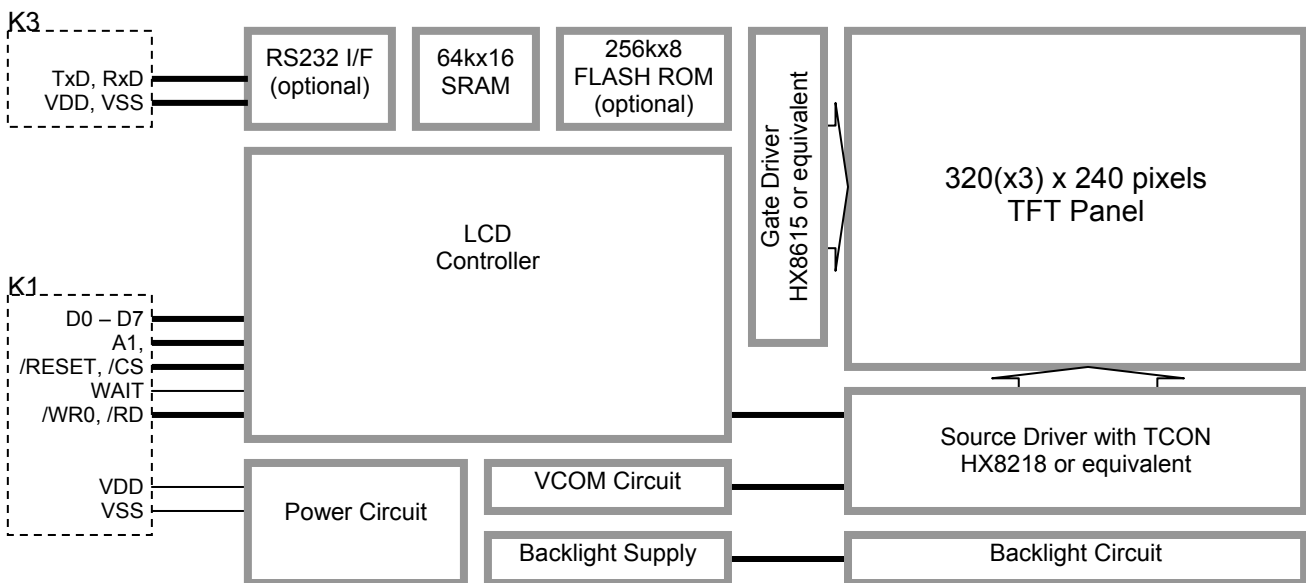
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1. General Specification

Display Technology :	a-Si TFT active matrix
Display Mode :	TN Type Full Color / Transmissive / Normal White
Screen Size(Diagonal) :	5.7"
Outline Dimension :	155.2 x 109.0 x 12.7 MAX. (mm) (see attached drawing for details)
Active Area :	115.2 x 86.4 (mm)
Number of dots :	320 x 3 (RGB) x 240
Dot Pitch :	0.12 x 0.36 (mm)
Pixel Configuration :	RGB Stripe
Backlight :	LED
Surface Treatment :	Anti-Glare Treatment
Viewing Direction :	12 o'clock
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

2. Block Diagram



2.1 Terminal Functions

2.1.1 MCU Terminal (K1, 8bit-Data, 1bit-Add)

Pin No.	Pin Name	I/O	Descriptions
1	VSS	Power Input	Power Supply GND (0V)
2			
3	VDD	Power Input	Positive Power Supply
4			
5	A1	Input	Register Select A1=LOW: Accessing Address F004 (command package port) A1=High: Accessing Address F006 (data and status port)
6	/CS	Input	Chip Select Inputs /CS=LOW: Data IO is enabled
7	/RESET	Input	Reset Signal Input /RESET=LOW: Reset /RESET=HIGH: Normal
8	D0	Bi-directional I/O	8-bit bi-directional data bus
:	:		
15	D7		
16	WAIT	Output	Wait Signal
17	/RD	Input	Read enable input, active LOW
18	/WR0	Input	Write enable input, active LOW
19	NC	-	No connection, leave open
20	NC	-	No connection, leave open

2.1.2 RS232 Terminal (K3)

Pin No.	Pin Name	I/O	Descriptions
1,2	Tx	Output	Data Output (to pin2 of PC RS232C<9pin D-connector>)
3,4	Rx	Input	Data Input (to pin3 of PC RS232C<9pin D-connector>)
5,6	VSS	Power	Power (0V) and Signal ground (to pin5 of PC RS232C<9pin D-connector>)
7,8	NC	-	No connection, leave open
9,10	VDD	Power	Positive Power Supply

3. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Supply Voltage	V_{DD}	-0.3	5.5	V	$V_{SS} = 0V$
Input Voltage	V_{IN}	-0.3	5.5	V	$V_{SS} = 0V$
Operating Temperature	T_{OP}	-20	70	°C	No Condensation
Storage Temperature	T_{ST}	-30	80	°C	No Condensation

Cautions:

Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

4. Electrical Characteristics

4.1 DC Characteristics (MCU terminal)

$V_{SS}=0V, V_{DD} = 5.0V, T_{OP} = 25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Voltage	V_{DD}	4.8	5.0	5.2	V	VDD
Input High Voltage	V_{IH}	3.0	-	VDD	V	Input pins, Bi-direction pins
Input Low Voltage	V_{IL}	VSS	-	0.6	V	Input pins, Bi-direction pins
Output High Voltage	V_{OH}	2.6	-	-	V	Bi-direction pins (*1)
Output Low Voltage	V_{OL}	-	-	0.6	V	Bi-direction pins (*2)
Operating Current	I_{DD}	-	260	600	mA	VDD

Note:

*1. $I_{OH} = -3.0mA$

*2. $I_{OL} = 3.0mA$

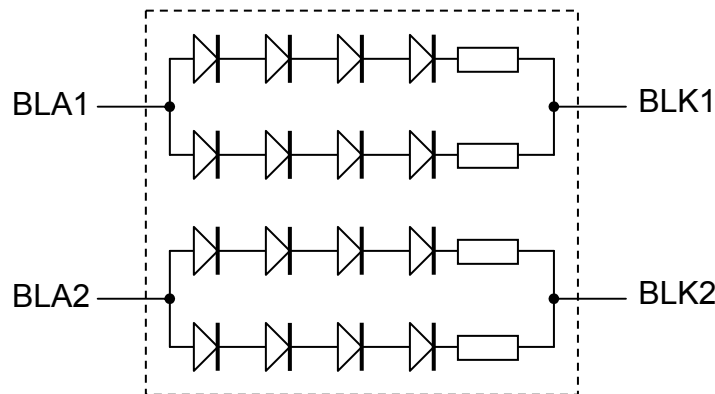
4.2 LED Backlight Circuit Characteristics

$V_{BLK1}=V_{BLK2}= 0V, I_{f_{BLA1}}+I_{f_{BLA2}}=60mA, T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Note
Forward Voltage	$V_{f_{BLA}}$	-	12.4	-	V	BLA1, BLA2
Forward Current	$I_{f_{BLA}}$	-	-	100	mA	BLA1+BLA2
Life Time	-	-	20000	-	hr	
Uniformity	-	75	80	-	%	

Cautions:

Exceeding the recommended driving current could cause substantial damage to the backlight and shorten its lifetime.



No. of LED = 4x4=16 pcs

4.3 AC Characteristics

Please refer to LCD controller datasheet for details.

5. Optical Characteristics

Light source: C light, using CMO TN LC + Polarizer reference only

Item	Symbol	MIN.	TYP.	MAX.	UNIT	Note.
Brightness	-	200	250	-	nit	
Transmittance	Tr		8.6	-	%	
Contrast Ratio	CR	150	250	-	-	(*1)
White Color Chromaticity(X)	W _X	0.282	0.313	0.342	-	
White Color Chromaticity(Y)	W _Y	0.299	0.338	0.359	-	
Response Time Rise	T _R	-	15	30	ms	
Response Time Fall	T _F	-	35	50	ms	
Viewing Angle(Φ=180°)	θ _l	-	15	-	deg	CR≥10 (*2)
Viewing Angle(Φ=0°)	θ _r	-	45	-	deg	CR≥10 (*2)
Viewing Angle(Φ=90°)	θ _u	-	15	-	deg	CR≥10 (*2)
Viewing Angle(Φ=270°)	θ _d	-	35	-	deg	CR≥10 (*2)
NTSC Ratio	S	-	50%	-	-	

Note:

***1. Definition of Contrast Ratio**

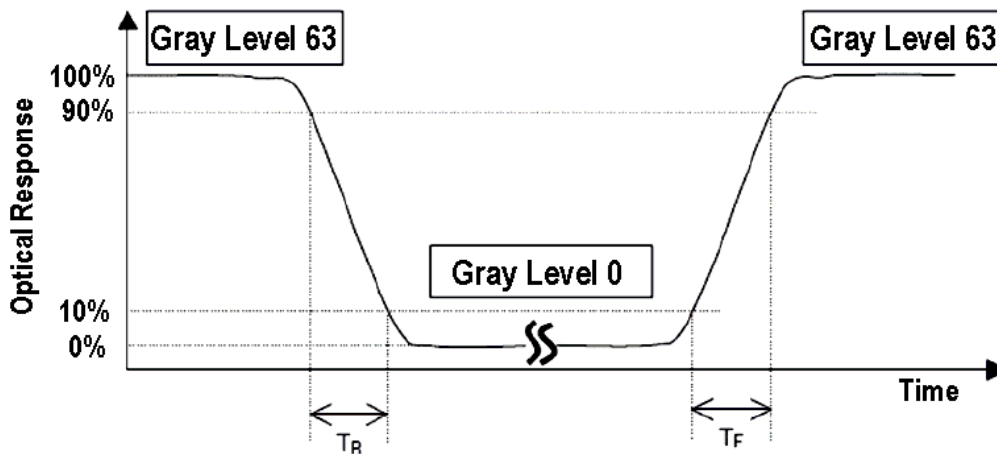
The contrast ratio could be calculate by the following expression:

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

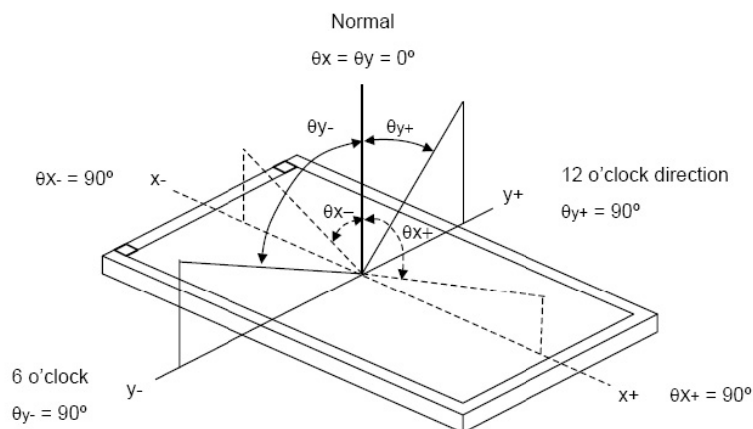
Where : L₆₃=Luminance of gray level 63

L₀=Luminance of gray level 0

CR=CR at middle point of the LCD panel.



***2 Definition of Viewing Angle**



6. Function Specifications

6.1 Hard-wired Setting

The following is the list of Jumpers on the LCD module:

Note: Never try to change the reserved jumper. It may damage the system

Interface Mode	interface terminal	JP1	JP3	JP4, JP5	JP25	JP26	JP27	Note
8bit-data 1bit-address	K1	OPEN	CLOSE	OPEN	OPEN	CLOSE	OPEN	Default setting
RS232C interface	K3	OPEN	CLOSE	OPEN	CLOSE	CLOSE	OPEN	

6.2 VR setting

P6, P4 adjust the VCOM signal on K5 (LCD terminal).

Check point: C12-positive terminal to GND

VCOM should be swing between +3.5V and -1.5V (typ.)

Note,

as VCOM signal generated by POL signal form LCD module, it must connect the LCD module for the adjustment.

P5 adjust the VGL, output on K5 (LCD terminal).

Check-point: C15-negative terminal to GND

VGL should be -10V(typ.)

Note,

the power supply is controlled by display power on command. it must init the controller for the adjustment

6.3 Command Packet Format

All commands are organized in packet with a 1 byte “Opcode” followed by optional parameters / data up to 64 bytes.

6.3.1 Command Packet Format

Opcode (1 byte)	Parameters / Data (up to 64 bytes)
-----------------	------------------------------------

For multi-byte parameter/data, send LSB (low byte)first, MSB (highest byte) last.

6.3.2 Opcode Group

- 00 - 0F Reserved for Serial Communication
- 10 - 1F 2D Hardware-acceleration: Fonts Drawing Operations
- 20 - 2F 2D Hardware-acceleration: Geometric Drawing Operations
- 30 - 3F Audio Operations
- 40 - 4F Reserved
- 50 - 5F Reserved
- 60 - 6F Communication
- 70 - 7F Reserved
- 80 - 8F System Control
- F0 – FF Reserved for serial mode synchronization

6.3.3 Opcode Description

Opcode (HEX)	Operations	Parameters / Data
00	Set “Control & Status Port” of the Command Interpreter	The value of this data (one byte) will be directly written to the Control & Status register.
10	charset_config	Character Set (1 byte): 00: Built in 8x8 ASCII 01: 8x8 CGRAM (Embedded RAM) 02: 8x16 CGRAM (Embedded RAM) 03: 16x16 CGRAM (Embedded RAM) 04: 16x16 GB2312-80 (External ROM) 05: 16x16 BIG5 (External ROM) 06: 8x8 Custom 8-bit encoding (External ROM) 07: 8x8 Custom 16-bit encoding (External ROM)
12	set_print_coord	Character Print Coordinates (4 bytes) - x (2 bytes) - y (2 bytes) For Mono LCD, x = (multiple of 8) – 1 For Color LCD, no restriction on the value of x coordinate
14	set_font_fgcolor	Character Foreground Color (2 bytes) (same as td_fgcolor, with opcode = (20 HEX)) Mono LCD: 1bpp, 2bpp, 4bpp Color LCD: 16-bit TFT (5R:6G:5B) 12-bit STN (4R:4G:4B)
15	set_font_bgcolor	Character Background Color (2 bytes) Mono LCD: 1bpp, 2bpp, 4bpp Color LCD: 16-bit TFT (5R:6G:5B) 12-bit STN (4R:4G:4B)
16	show_char	Display Character (1 or 2 bytes)
17	show_string	Display String - Character count (1 byte) (0 ≤ character count ≤ 63) - String (≤ 63 bytes)

Opcode (HEX)	Operations	Parameters / Data																
20	td_fgcolor	Set Foreground Color (2 bytes) Mono LCD: 1bpp, 2bpp, 4bpp Color LCD: 16-bit TFT (5R:6G:5B) 12-bit STN (4R:4G:4B)																
23	draw_pixel	Draw Pixel - x (2 bytes) - y (2 bytes)																
24	draw_line	Draw Line - x_start (2 bytes) - y_start (2 bytes) - x_end (2 bytes) - y_end (2 bytes)																
26	draw_rect	Draw Hollow Rectangle (Box) - x_start (2 bytes) - y_start (2 bytes) - x_end (2 bytes) - y_end (2 bytes)																
27	fill_rect	Fill Rectangle (Box) - x_start (2 bytes) - y_start (2 bytes) - x_end (2 bytes) - y_end (2 bytes)																
28	draw_circle	Draw Circle - x_center (2 bytes) - y_center (2 bytes) - radius (1 byte)																
29	fill_circle	Fill Circle - x_center (2 bytes) - y_center (2 bytes) - radius (1 byte)																
60	set_baud	Set baud rate - divisor (lower byte) (1 byte) - divisor (upper byte) (1 byte) <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Divisor</th> <th>RS232 baud rate</th> </tr> </thead> <tbody> <tr> <td>1047</td> <td>110</td> </tr> <tr> <td>24</td> <td>4800</td> </tr> <tr> <td>12</td> <td>9600 <default></td> </tr> <tr> <td>6</td> <td>19200</td> </tr> <tr> <td>3</td> <td>38400</td> </tr> <tr> <td>2</td> <td>57600</td> </tr> <tr> <td>1</td> <td>115200</td> </tr> </tbody> </table>	Divisor	RS232 baud rate	1047	110	24	4800	12	9600 <default>	6	19200	3	38400	2	57600	1	115200
Divisor	RS232 baud rate																	
1047	110																	
24	4800																	
12	9600 <default>																	
6	19200																	
3	38400																	
2	57600																	
1	115200																	
80	refresh_setting	N/A																
81	set_mem_ptr	Set memory pointer - address (3 bytes)																
82	read_reg	Read register - address (2 bytes)																
83	write_reg	Write register - address (2 bytes) - data (1 byte)																
84	write_mem	Write memory - count (1 byte) - data (up to 63 bytes)																
8F	mem_clk_en	Enable memory clock "69 45 61 67 6C 65" (6 bytes in HEX)																

6.3.4 Registers Table

Register (HEX)	R/W	Reset Value	Descriptions
F000	Read Write	1000 0000	Chip ID Port Always read back <u>80 (HEX)</u> Write "DE FC 0B" (HEX) to enable memory clock, same as command with OPCODE "8F".
F001	Read only	0000 0000	Chip Revision Port Always read back <u>00 (HEX)</u> for iEM8000
F004	Write only	-	Command Packet Port - Writing of Command Packets.
F006	Write	xxxx 1xx0	Port for writing control or reading status Bit[7:4] : Reserved Bit[3] : DISPLAY ON / OFF 0=DISPLAY ON 1=DISPLAY OFF Bit[2:1] : Reserved Bit[0] : End of Command, Write "1" after each command packet
	Read	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : FIFO full Read "1" if Command FIFO is full. Hosts must read this bit = "0" before writing to Command Packet Port.
F080	Read / Write	0000 0000	Bit[7:6] : External SRAM Select Bit[7:6] = 11: Required setting - 64Kx16 external SRAM connected Bit[5] : Horizontal TFT Pulse Polarity 0: Active low 1: Active high Bit[4] : Vertical TFT Pulse Polarity 0: Active low 1: Active high Bit[3] : STN Panel I/F Data Width 0: 4-bit single 1: 8-bit single Bit[2] : Color Mode Select 0: Monochrome 1: Color Bit[1:0] : Color Depth Select If Monochrome (Bit[2] = 0) 00: 1 bit-per-pixel 01: 2 bit-per-pixel 10: 4 bit-per-pixel 11: Reserved If Color (Bit[2] = 1) 00: 16 bit-per-pixel (TFT panel) 01: 12 bit-per-pixel (CSTN panel) 10: Reserved 11: Reserved
F081	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Panel Horizontal Character Count – 1, Panel Horizontal Character Count[8:0] supports horizontal panel size up to 128 characters or 1024 pixels.
F082	Read / Write	0000 0000	Bit[7:0] : Panel Line Count - 1 bit[7:0]
F083	Read / Write	xxxx xxx0	Bit[7:1] : Reserved Bit[0] : Panel Line Count – 1 bit[8], Panel Line Count[8:0] supports vertical panel size up to 512 lines.
F084	Read / Write	0000 0000	Bit[7:0] : Display Start Position X Coordinate – 1 bit[7:0]
F085	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position X Coordinate – 1 bit[9:8]

Register (HEX)	R/W	Reset Value	Descriptions
F086	Read / Write	0000 0000	Bit[7:0] Display Start Position Y Coordinate – 1 bit[7:0]
F087	Read / Write	xxxx xx00	Bit[7:2] : Reserved Bit[1:0] : Display Start Position Y Coordinate – 1 bit[9:8] Display Start Position (X,Y) is for panning of the view port on a virtual display.
F088	Read / Write	0000 0000	LCD_LUT1 Bit[7:4] : for Gray level 3 Bit[3:0] : for Gray level 2
F089	Read / Write	0000 0000	LCD_LUT0 Bit[7:4] : for Gray level 1 Bit[3:0] : for Gray level 0
F08A	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Virtual Display Character count – 1 It supports horizontal virtual size up to 128 characters or 1024 pixels.
F08B	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : WF count for STN panels 000000: WF pin toggles every frame 000001: WF pin toggles every 2 LP pulses 000010: WF pin toggles every 3 LP pulses 111111: WF pin toggles every 64 LP pulses
F08C	Read / Write	xxxx 0000	Bit[7:4] : Reserved Bit[3:0] : Horizontal non-display period 0000: 2 characters (16 pixels) 0001: 3 characters (24 pixels) 1111: 17 characters (136 pixels)
F08D	Read / Write	xxxx 0000	Bit[7:4] : Reserved Bit[3:0] : Vertical non-display period 0000: 1 line 0001: 2 lines 1111: 16 lines
F08E	Read / Write	0000 000x	Bit[7:4] : Pixel Clock Divider 0000: 24 MHz (divided by 1) 0001: 12 MHz (divided by 2) 0010: 8 MHz (divided by 3) 0011: 6MHz (divided by 4) 1111: 1.5MHz (divided by 16) Bit[3] : Display Blank 0: Normal 1: Blank Bit[2] : Display Invert 0: Normal 1: Invert Bit[1] : LCD_ON Polarity 0: LCD_ON pin active low 1: LCD_ON pin active high Bit[0] : Reserved

Register (HEX)	R/W	Reset Value	Descriptions
F08F	Read / Write	x000 0000	Bit[7] : Reserved Bit[6:0] : Number of frames to start – 1 Maximum 128 frames (see section 2.15.1 for detail)
F090	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Front Porch for TFT panels 000000: 1 pixel 000001: 2 pixels 111111: 64 pixels
F091	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Horizontal Back Porch for TFT panels 000000: 1 pixel 000001: 2 pixels 111111: 64 pixels
F092	Read / Write	xxx0 0000	Bit[7:5] : Reserved Bit[4:0] : Horizontal Pulse Width for TFT panels 00000: 1 pixel 00001: 2 pixels 11111: 32 pixels
F093	Read / Write	0000 0000	Bit[7:0] : Scratch Pad register
F094	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Front Porch for TFT panels 000000: 1 line 000001: 2 lines 111111: 64 lines
F095	Read / Write	xx00 0000	Bit[7:6] : Reserved Bit[5:0] : Vertical Back Porch for TFT panels 000000: 1 line 000001: 2 lines 111111: 64 lines
F096	Read / Write	xxx0 0000	Bit[7:5] : Reserved Bit[4:0] : Vertical Pulse Width for TFT panels 00000: 1 line 00001: 2 lines 11111: 32 lines

Register (HEX)	R/W	Reset Value	Descriptions
F100	Read / Write	00xx xx00	<p>Bit[7] – Enable / Disable 0: Disable Sprite 1: Enable Sprite</p> <p>Bit[6] – Transparency 0: Transparency disable 1: Transparency enable When enabled: Sprite data = 00 becomes transparent and LCD background will be displayed instead.</p> <p>Bit[5:2] – Reserved</p> <p>Bit[1:0] – Sprite Modes Select 01: Sprite with 2 bit-per-pixel 00, 10, 11: Reserved</p>
F102	Read / Write	0000 0000	Bit[7:0] - SP_LUT0L[7:0]
F103	Read / Write	0000 0000	Bit[7:0] - SP_LUT0H[7:0]
F104	Read / Write	0000 0000	Bit[7:0] - SP_LUT1L[7:0]
F105	Read / Write	0000 0000	Bit[7:0] - SP_LUT1H[7:0]
F106	Read / Write	0000 0000	Bit[7:0] - SP_LUT2L[7:0]
F107	Read / Write	0000 0000	Bit[7:0] - SP_LUT2H[7:0]
F108	Read / Write	0000 0000	Bit[7:0] - SP_LUT3L[7:0]
F109	Read / Write	0000 0000	Bit[7:0] - SP_LUT3H[7:0]
F10A	Read / Write	0000 0000	Bit[7:0] – Sprite Horizontal Pixel Count – 1 Maximum 256 pixels
F10B	Read / Write	0000 0000	Bit[7:0] – Sprite Vertical Line Count – 1 Maximum 256 lines
F10C	Read / Write	0000 0000	Bit[7:0] – Sprite Horizontal Start Position bit[7:0]
F10D	Read / Write	xxxx xx00	<p>Bit[7:2] – Reserved</p> <p>Bit[1:0] - Sprite Horizontal Start Position bit[9:8] Sprite Horizontal Start Position bit[9:0] is measured in pixels and counted from left to right of the edge of the panel display (i.e. not virtual display).</p>
F10E	Read / Write	0000 0000	Bit[7:0] – Sprite Vertical Start Position bit[7:0]
F10F	Read / Write	xxxx xxx0	<p>Bit[7:1] – Reserved</p> <p>Bit[0] - Sprite Vertical Start Position bit[8] Sprite Vertical Start Position bit[8:0] is measured in lines and counted from top to bottom of the edge of the panel display (i.e. not virtual display).</p>
F142	Write Only	0000 0000	Bit[7:0] – Sprite / overlay storage starting address bit[7:0]
F143	Write Only	0000 0000	Bit[7:0] – Sprite / overlay storage starting address bit[15:8]
F144	Write Only	0000 0000	<p>Bit[7:2] – Reserved</p> <p>Bit[1:0] – Sprite / overlay storage starting address bit[17:16] This is the starting address to put the sprite/overlay image</p>
F180	Read Only	0000 0000	Bit[7:0] – Background Color bit[7:0]
F181	Read Only	0000 0000	Bit[7:0] –Background Color bit[15:8]
F182	Read Only	0000 0000	Bit[7:0] – Foreground Color bit[7:0]
F183	Read Only	0000 0000	Bit[7:0] –Foreground Color bit[15:8]

Register (HEX)	R/W	Reset Value	Descriptions
F500	Read / Write	1110 1110	CS0 Configuration Port – Pulse Width <u>Bit[7:4]</u> : Write Cycle Pulse Width 0000: 1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks 1110:15 memory clocks 1111: Reserved <u>Bit[3:0]</u> : Read Cycle Pulse Width 0000: 1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks 1110:15 memory clocks 1111: Reserved
F501	Read / Write	0000 0000	CS0 Configuration Port – Control <u>Bit[7]</u> : Enable bit 0:Disable CS0 1:Enable CS0 <u>Bit[6]</u> : Memory data bus width 0: 8-bit memory data bus width 1: 16-bit memory data bus width <u>Bit[5]</u> : 16-bit SRAM option 0:two 8-bit SRAMs 1:one 16-bit SRAM <u>Bit[4]</u> : Reserved <u>Bit[3]</u> : CS0 assertion time relative to address assertion. 0:CS0 and address assert at the same time 1:CS0 lags address by 1 memory clock. <u>Bit[2]</u> : CS0 Negation Timing 0:CS0 and Address negate at the same time 1:CS0 leads Address by 1 memory clock in write access. <u>Bit[1]</u> : Write Enable Assertion Time 0: Write Enable and Address Assert at the same time. 1: Write Enable lags Address by 1 memory clock. <u>Bit[0]</u> : Write Enable Negation Time 0: Write Enable and Address negate at the same time. 1: Write Enable leads Address by 1 memory clock.
F504	Read / Write	xxxx 1110	CS1 Configuration Port – Pulse Width <u>Bit[7:4]</u> : Reserved <u>Bit[3:0]</u> : Read Cycle Pulse Width 0000: 1 memory clock (24 MHz -> 41.6ns) 0001: 2 memory clocks 0011: 3 memory clocks 1101:14 memory clocks 1110:15 memory clocks 1111: Reserved
F505	Read / Write	0000 0000	CS1 Configuration Port – Control <u>Bit[7]</u> : Enable bit 0:Disable CS1 1:Enable CS1 <u>Bit[6]</u> : Memory data bus width 0: 8-bit memory data bus width 1: 16-bit memory data bus width <u>Bit[5]</u> : Reserved <u>Bit[4]</u> : Reserved <u>Bit[3]</u> : CS1 assertion time relative to address assertion. 0:CS1 and Address assert at the same time 1:CS1 lags Address by 1 memory clock. <u>Bit[2]</u> : CS1 Negation Timing 0:CS1 and Address negate at the same time 1:CS1 leads Address by 1 memory clock in write access. <u>Bit[1:0]</u> : Reserved
F6C4	Read / Write	xx11 0011	Set Memory Clock Divide <u>Bit[7:6]</u> = Reserved <u>Bit[5:0]</u> = 010000 to set 24MHz memory clock for proper operations

6.4 UART Serial Host Communication Packet Format

In UART serial host mode, each communication packet starts with a byte of “FF” and ended with “FE”. Length of parameters (one byte) is also required into the packet. An Acknowledge Packet will be sent back to the UART serial host by the T8000 once the command is finished execution.

UART Serial host Communication Packet Format

Sequence	No of byte	Content
1	1	0xFF (hex) <START BYTE>
2	1	Opcode
3	1	Length of Parameters
4	1 to 64	Parameters / Data (up to 64bytes)
5	1	0xFE (hex) <END BYTE>

Note: A “FF” bytes sequence of length equal to or more than 65 will cause re-synchronization.

UART Serial host re-synchronization Packet Format

Sequence	No of byte	Content
1	Equal or more than 65	0xFF (hex)
2		0xFF (hex)
:		:
:		:

Note: A “FF” bytes sequence of length equal to or more than 65 will cause re-synchronization.

For commands required read data (Opcode 82) from the T8000, it will send read data embedded in the Acknowledge Packet automatically when data is ready.

UART Serial host Acknowledge Packet Format, without “register read data”

Sequence	No of byte	Content
1	1	0x00 (hex)

UART Serial host Acknowledge Packet Format, with “register read data”

Sequence	No of byte	Content
1	1	Register read data
2	1	0x00 (hex)

7. Precautions of using LCD Modules

Mounting

- Mounting must use holes arranged in four corners or four sides.
- The mounting structure so provide even force on to LCD module. Uneven force (ex. Twisted stress) should not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- It is suggested to attach a transparent protective plate to the surface in order to protect the polarizer. It should have sufficient strength in order to the resist external force.
- The housing should adopt radiation structure to satisfy the temperature specification.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. Never rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics deteriorate the polarizer.)
- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer

Operating

- The spike noise causes the mis-operation of circuits. It should be within the $\pm 200\text{mV}$ level (Over and under shoot voltage)
- Response time depends on the temperature.(In lower temperature, it becomes longer.)
- Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- When fixed patterns are displayed for a long time, remnant image is likely to occur.
- Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference

Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

Storage

When storing modules as spares for a long time, the following precautions are necessary.

- Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

Protection Film

- When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to be main on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.
- When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

Transportation

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

8. Appendix A <Inspection items and criteria for appearance defect>

Items	Criteria			
Open Segment or Common	Not permitted			
Short	Not permitted			
Wrong Viewing Angle	Not permitted			
Decliners	Not permitted			
Contrast Ration Uneven	According to the limit specimen			
Crosstalk	According to the limit specimen			
White spots	X>1 pixel	A-area	Not permitted	Max 6 spots allowed
		B-area	Max. 1 allowed	
	1/2 pixel<X≤1 pixel	A-area	Not permitted	
		B-area	Max. 2 allowed	
	X≤1/2 pixel	A-area	Max. 1 allowed	
		B-area	Max. 4 allowed	
Black Sport	X>1 pixel	A-area	Not permitted	
		B-area	Max. 2 allowed	
	X≤1/2 pixel	A-area	Max. 1 allowed	
		B-area	Max. 4 allowed	
Line Defect	Apparent vertical horizontal line defects are not permitted			

Note:

1. On Pixel include 3 dots (RedDot + GreenDot + BlueDot)
2. Definition of Panel "A-area" and "B-area"

