



**TOPWAY displays**

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# LMT056DIDFWD-ABB

## LCD Module User Manual

Prepared by:	Checked by:	Approved by:
Date:	Date:	Date:

Rev.	Descriptions	Release Date
0.1	Preliminary new release	2012-08-01
0.2	Add on Touch Panel Controller	2012-11-08
0.3	Typing Correction on Terminal Function	2012-11-15

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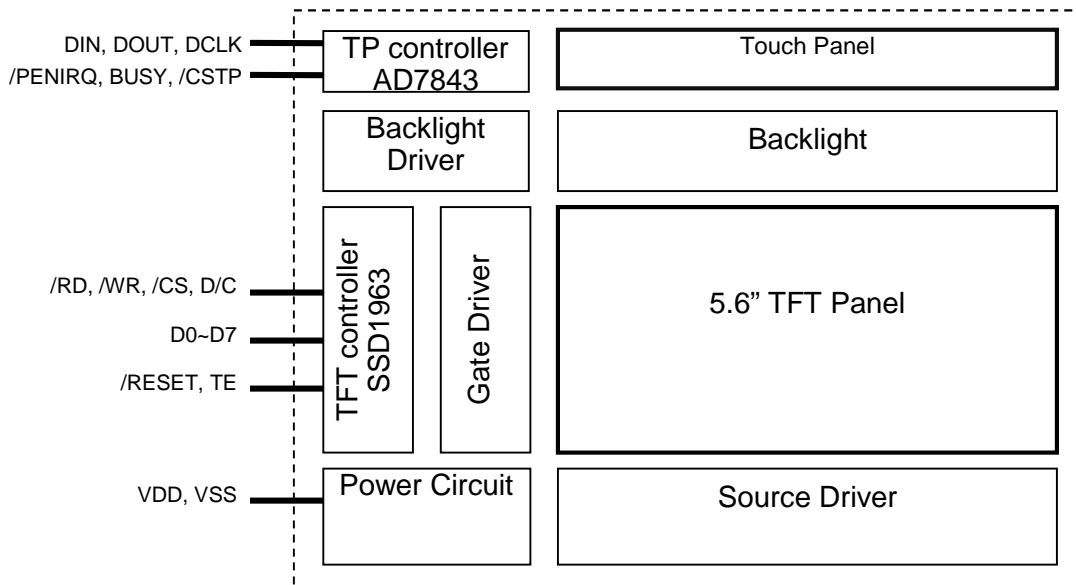
**1. Product Highlight**

- Power Supply and logic level
  - 5.0V supply
  - 3.3V logic level(tolerate 5.0V input)
- Display
  - TFT LCD display
  - 640 x 480 pixels
  - 65536colors
  - data refresh rate 20fps possible
- Host Interface
  - 8bit data, 1bit address, 8080mode
  - fast command execution
- Built-in Drawing Engine
  - Hardware rotation of 0°,90°,180°,270°
  - Hardware Display Mirroring
  - Hardware Windowing
  - Address auto increment
- Backlight Control
  - 256 level backlight brightness control
- Touch Panel
  - 4 wire resistive touch panel

**General Specification beat**

Signal Interface :	8bit data, 1bit address
Display Technology :	TFT active matrix
Display Mode :	Transmissive / Normal White
Screen Size(Diagonal) :	5.6"
Outline Dimension :	155.2 x 109.0 x 14.2 (mm) (see attached drawing for details)
Active Area :	112.896 x 84.672 (mm)
Number of dots :	640 x 3 (RGB) x 480
Pixel Pitch :	0.0588 x 0.1764 (mm)
Pixel Configuration :	RGB Stripe
Backlight :	LED
Color Depth:	1677216(24bit)colors
Surface Treatment:	Anti-Glare Treatment
Viewing Direction :	12 o'clock
Operating Temperature :	-20 ~ +70°C
Storage Temperature :	-30 ~ +80°C

**2. Block Diagram**



### 3. Terminal Function (Input Terminal)

No.	Pin Name	I/O	Descriptions
1	VSS	P	Power Supply GND (0V)
2			
3	VDD	I	Positive Power Supply (5.0V)
4			
5	D/C	I	Register Select D/C=0, command D/C=1, data or parameter
6	/CS	I	Chip Select signal
7	/RESET	I	Reset signal, /RESET=1, normal /RESET=0, reset execute
8	D0	I/O	8bit Data bus
:	:		
15	D7		
16	TE	O	Tear Signal (*1)
17	/RD	I	Read Status signal
18	/WR	I	Write signal
19	NC	-	No Connection
20	NC	-	No Connection
21	/PENIRQ	I	Pen Interrupt (*2)
22	DOUT	O	Data Output
23	BUSY	O	Busy Output
24	DIN	I	Data Input
25	/CSTP	I	Chip Select, also for initiating the conversions
26	DCLK	I	Clock Input for Serial Data & conversions
27	NC	-	No Connection
28	VSS	P	Power Supply GND (0V)

Note.

\*1. Tear signal may leave open when not use

\*2. Pulled-up by internal resistor

## 4. Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit	Condition
Power Supply voltage	$V_{DD}$	-0.3	6.0	V	
Backlight Supply voltage	$V_{DD\_BL}$	-0.3	6.0	V	
Operating Temperature	$T_{OP}$	-20	70	°C	No Condensation
Storage Temperature	$T_{ST}$	-30	80	°C	No Condensation

Note:

- \*1. This rating applies to all parts of the module. And should not be exceeded.
- \*2. The operating temperature only guarantees operation of the circuit. The contrast, response speed, and the other specification related to electro-optical display quality is determined at the room temperature,  $T_{OP}=25^{\circ}C$
- \*3. Ambient temperature when the backlight is lit (reference value)
- \*4. Any Stresses exceeding the Absolute Maximum Ratings may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

## 5. Electrical Characteristics

### 5.1 DC Characteristics

$V_{DD}=5.0V, T_{op}=25^{\circ}C, V_{SS}=0V$

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage	$V_{DD}$	4.8	5.0	5.5	V	*2
Input logic high voltage	$V_{IH}$	3.0	-	$V_{DD}$	V	*2, *3
Input logic low voltage	$V_{IL}$	0	-	0.6	V	*2, *3
Output logic high voltage	$V_{OH}$	3.0	-	3.6	V	*2, *3
Output logic low voltage	$V_{OL}$	0	-	0.6	V	*2, *3
Logic Supply Current (VDD)	$I_{DD}$	-	380.0	-	mA	Backlight (100%PWM)
		-	250.0	-	mA	Backlight (66%PWM)

Note:

- \*1. Never Apply logic signal before the VDD supply.
- \*2. VDD setting should match the signals voltage
- \*3. For all the inputs signals
- \*4. PLL Clock Freq=200MHz

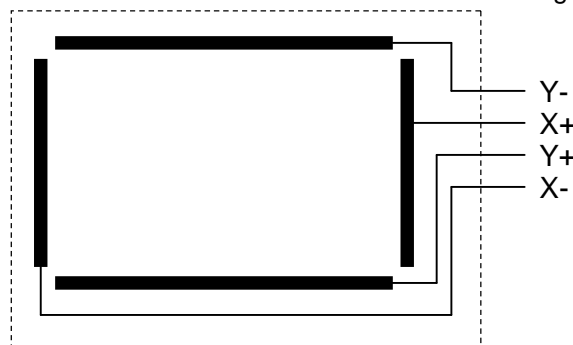
### 5.2 Touch Panel Characteristics

$T_{OP}=25^{\circ}C$

Items	Symbol	MIN.	TYP.	MAX.	Unit	Applicable Pin
Operating Force	Fop	60	-	100	g	-
Life Time	TL	-	1,000,000	-	times	-

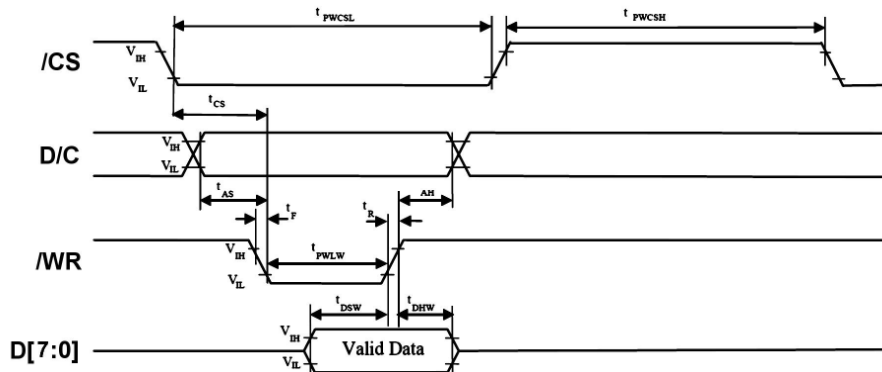
Cautions:

Exceeding the recommended Condition could cause substantial damage to the touch panel and shorten its lifetime.

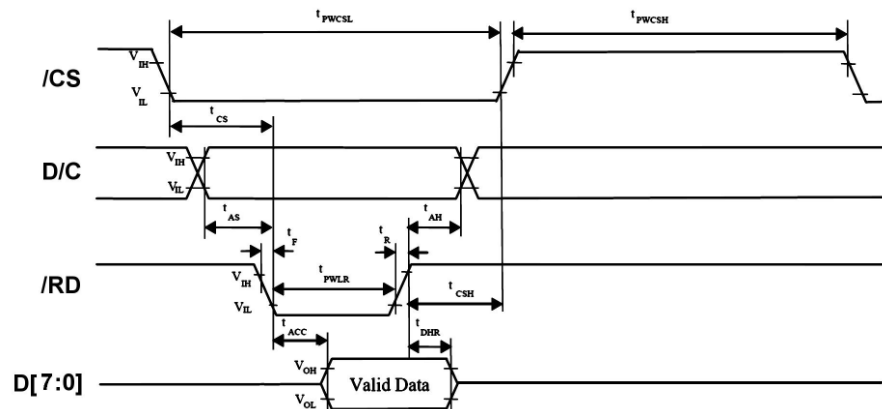


## 6. AC Characteristics

### 6.1 TFT Controller Timing Characteristics



8080 Mode Write Timing



8080 Mode Read Timing

$V_{SS}=0V, V_{DD}=5.0V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
System Clock Period(*1)	$t_{MCLK}$	$1/f_{MCLK}$	-	-	ns
Control Pulse High Width	$t_{PWCSL}$	Write	29	$1.5*t_{MCLK}$	ns
		Read	51	$1.3*t_{MCLK}$	ns
Control Pulse Low Width	$t_{PWCSH}$	Write (next write cycle)	29	$1.5*t_{MCLK}$	ns
		Write (next read cycle)	113	$9*t_{MCLK}$	ns
		Read	113	$9*t_{MCLK}$	ns
Address Setup Time	$t_{AS}$	7.8	-	-	ns
Address Hold Time	$t_{AH}$	9	-	-	ns
Write Data Setup Time	$t_{DSW}$	11.5	-	-	ns
Write Data Hold Time	$t_{DHW}$	7.8	-	-	ns
Write Low Time	$t_{PWLW}$	28	-	-	ns
Read Data Hold Time	$t_{DHR}$	9.1	-	-	ns
Access Time	$t_{ACC}$	63.3	-	-	ns
Read Low Time	$t_{PWL R}$	58	-	-	ns
Rise Time	$t_R$	-	-	0.4	ns
Fall Time	$t_F$	-	-	0.4	ns
Chip select setup time	$t_{CS}$	9	-	-	ns
Chip select hold time to read signal	$t_{CSH}$	9	-	-	ns

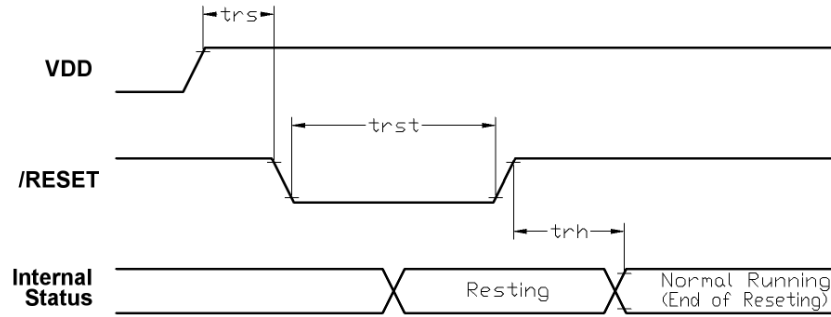
Note:

\*1.  $t_{MCLK}$  is the System Clock Period, which may config by internal PLL setting

\*2. LMT056DIDFWD is driving by external 10MHz, and clock up by enabling the SSD1963 internal PLL

\*3. Suggested PLL clock setting is 200MHz

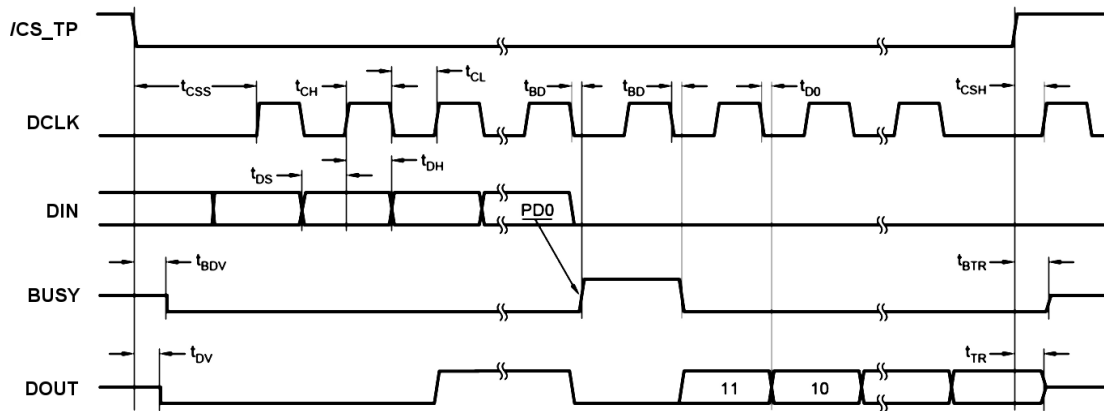
6.2 TFT Controller Reset Timing



$V_{SS}=0V, V_{DD}=5.0V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Reset setup time	trs	2	-	-	ms
Reset pulse	trst	0.2	-	-	ms
Reset hold time	trh	2	-	-	ms

6.3 Touch Panel Controller Timing Characteristics



$V_{SS}=0V, V_{DD}=3.3V, T_{OP}=25^{\circ}C$

Item	Symbol	MIN.	TYP.	MAX.	Unit
Acquisition Time	$t_{ACQ}$	1.9	-	-	us
DIN Valid Prior to DCLK Rising	$t_{DS}$	125	-	-	ns
DIN Hold After DCLK HIGH	$t_{DH}$	13	-	-	ns
DCLK Falling to DOUT Valid	$t_{DO}$	-	-	250	ns
/CS_TP Falling to DOUT Enabled	$t_{DV}$	-	-	160	ns
/CS_TP Rising to DOUT Disabled	$t_{TR}$	-	-	250	ns
/CS_TP Falling to First DCLK Rising	$t_{CSS}$	125	-	-	ns
/CS_TP Rising to DCLK Ignored	$t_{CSH}$	10	-	-	ns
DCLK HIGH	$t_{CH}$	250	-	-	ns
DCLK LOW	$t_{CL}$	250	-	-	ns
DCLK Falling to BUSY Rising	$t_{BD}$	-	-	250	ns
/CS_TP Falling to BUSY Enabled	$t_{BDV}$	-	-	160	ns
/CS_TP Rising to BUSY Disabled	$t_{BTR}$	-	-	250	ns

### 7. Optical Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	UNIT	Note.
Viewing angle (CR ≥ 10)	$\theta_L$	9 o'clock	60	70	-	degree	*2
	$\theta_R$	3 o'clock	60	70	-		
	$\theta_T$	12 o'clock	40	50	-		
	$\theta_B$	6 o'clock	60	70	-		
Response Time	$T_f$	Normal $\theta=0^\circ$	-	10	20	msec	*3
	$T_r$		-	15	30	msec	
Contrast ratio	CR		400	500	-	-	*1
Color chromaticlty	$W_X$		0.26	0.31	0.26	-	
	$W_Y$		0.28	0.33	0.38	-	
Luminance	L		-	350	-	cd/m <sup>2</sup>	*4
Luminance uniformity	$Y_U$		70	75	-	%	*4

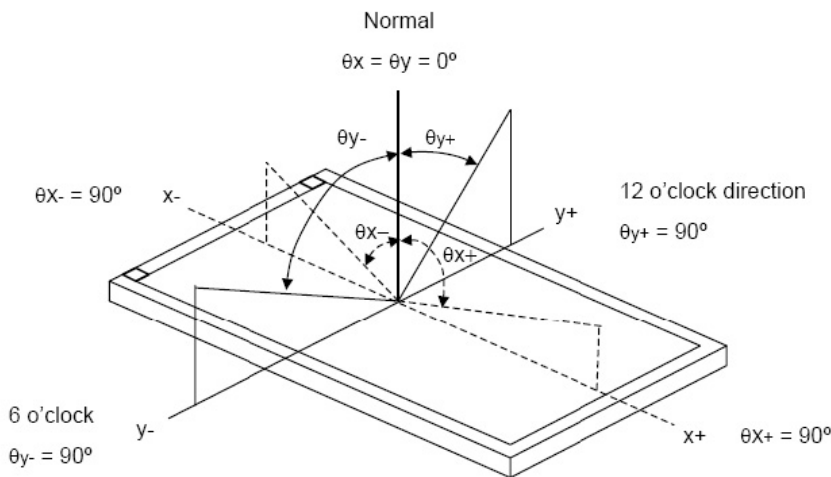
Note:

\*1. Definition of Contrast Ratio

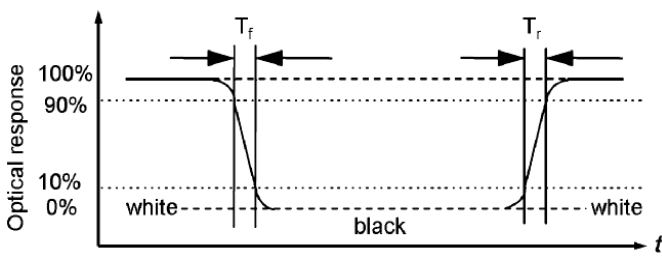
The contrast ratio could be calculate by the following expression:

Contrast Ratio (CR) = Luminanc with all pixels white / Luminance with all pixels black

\*2 Definition of Viewing Angle



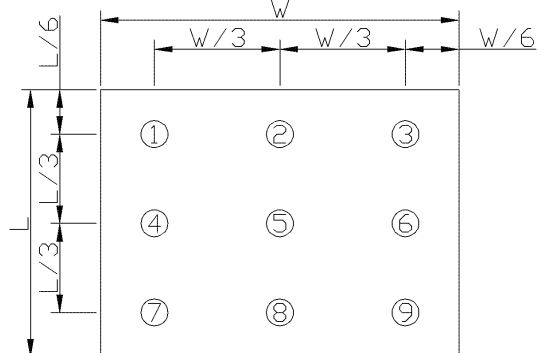
\*3 Definition of response time



\*4 Definition of Luminance Uniformity

Luminance uniformity (Lu)=

Min. Luminance form pt1~pt9 / Max Luminance form Pt1~pt9



\*5. Measured with TFT and backlight only

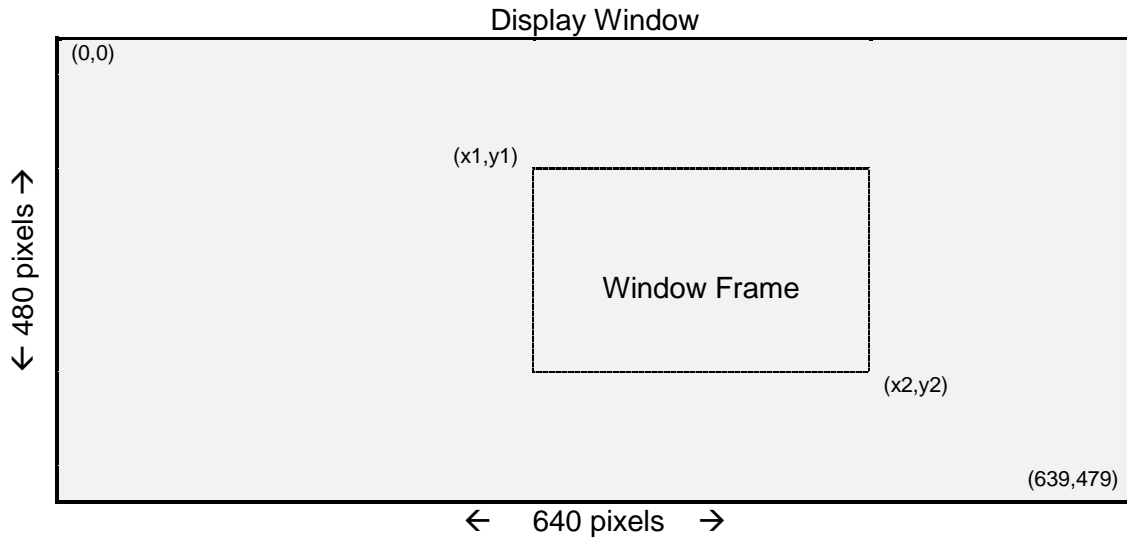


## 8. Function Specifications

### 8.1 TFT Controller Functions

#### 8.1.1 Display Memory Addressing

TFT module with 640x480 pixels, using SSD1963, address the display memory with a co-ordinate system as follow.



#### 8.1.2 Command Packet

- Command Packet organizes with “Command Code” followed by “Parameter”
- Command Code and Parameters are 8bit only
- Number of Parameters is depends on Command type  
some of the command followed with no parameter.

Seq.	D/C	/RD	/WR	Lo byte (D7:D0)
1	0	1	↑	Command code
2	1	1	↑	Parameter 1
3	1	1	↑	Parameter 2
4	1	1	↑	Parameter 3
:	:	:	:	:

#### 8.1.3 Data Format

- Display Data is in 24bit format (R:G:B=8:8:8)
- 24bit data built one pixels
- Display Data could be continue write (depends on command and configuration)

D/C	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0
1	1	↑	G7	G6	G5	G4	G3	G2	G1	G0
1	1	↑	B7	B6	B5	B4	B3	B2	B1	B0
1	1	↑	R7	R6	R5	R4	R3	R2	R1	R0
1	1	↑	G7	G6	G5	G4	G3	G2	G1	G0
1	1	↑	B7	B6	B5	B4	B3	B2	B1	B0
:	:	:	:	:	:	:	:	:	:	:

**8.1.4 Command Table**

Code (hex)	Command	Description
0x00	nop	No operation
0x01	soft_reset	Software Reset
0x0A	get_power_mode	Get the current power mode
0x0B	get_address_mode	Get the frame buffer to the display panel read order
0x0C	Reserved	Reserved
0x0D	get_display_mode	The SSD1963 returns the Display Image Mode.
0x0E	get_tear_effect_status	Get the Tear Effect status
0x0F	Reserved	Reserved
0x10	enter_sleep_mode	Turn off the panel. This command will pull low the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x11	exit_sleep_mode	Turn on the panel. This command will pull high the GPIO0. If GPIO0 is configured as normal GPIO or LCD miscellaneous signal with command set_gpio_conf, this command will be ignored.
0x12	enter_partial_mode	Part of the display area is used for image display.
0x13	enter_normal_mode	The whole display area is used for image display.
0x20	exit_invert_mode	Displayed image colors are not inverted.
0x21	enter_invert_mode	Displayed image colors are inverted.
0x26	set_gamma_curve	Selects the gamma curve used by the display panel.
0x28	set_display_off	Blanks the display panel
0x29	set_display_on	Show the image on the display panel
0x2A	set_column_address	Set the column address
0x2B	set_page_address	Set the page address
0x2C	write_memory_start	Transfer image information from the host processor interface to the SSD1963 starting at the location provided by set_column_address and set_page_address
0x2E	read_memory_start	Transfer image data from the SSD1963 to the host processor interface starting at the location provided by set_column_address and set_page_address
0x30	set_partial_area	Defines the partial display area on the display panel
0x33	set_scroll_area	Defines the vertical scrolling and fixed area on display area
0x34	set_tear_off	Synchronization information is not sent from the SSD1963 to the host processor
0x35	set_tear_on	Synchronization information is sent from the SSD1963 to the host processor at the start of VFP
0x36	set_address_mode	Set the read order from frame buffer to the display panel
0x37	set_scroll_start	Defines the vertical scrolling starting point
0x38	exit_idle_mode	Full color depth is used for the display panel
0x39	enter_idle_mode	Reduce color depth is used on the display panel.
0x3A	Reserved	Reserved
0x3C	write_memory_continue	Transfer image information from the host processor interface to the SSD1963 from the last written location
0x3E	read_memory_continue	Read image data from the SSD1963 continuing after the last read_memory_continue or read_memory_start
Hex Code	Command	Description
0x44	set_tear_scanline	Synchronization information is sent from the SSD1963 to the host processor when the display panel refresh reaches the provided scanline
0x45	get_scanline	Get the current scan line
0xA1	read_ddb	Read the DDB from the provided location
0xA8	Reserved	Reserved

8.1.5 Command Table(continue)

Code (hex)	Command	Description
0xB0	set_lcd_mode_	Set the LCD panel mode and resolution
0xB1	get_lcd_mode	Get the current LCD panel mode, pad strength and resolution
0xB4	set_hori_period	Set front porch
0xB5	get_hori_period	Get current front porch settings
0xB6	set_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0xB7	get_vert_period	Set the vertical blanking interval between last scan line and next LFRAME pulse
0xB8	set_gpio_conf	Set the GPIO configuration. If the GPIO is not used for LCD, set the direction. Otherwise, they are toggled with LCD signals.
0xB9	get_gpio_conf	Get the current GPIO configuration
0xBA	set_gpio_value	Set GPIO value for GPIO configured as output
0xBB	get_gpio_status	Read current GPIO status. If the individual GPIO was configured as input, the value is the status of the corresponding pin. Otherwise, it is the programmed value.
0xBC	set_post_proc	Set the image post processor
0xBD	get_post_proc	Set the image post processor
0xBE	set_pwm_conf	Set the image post processor
0xBF	get_pwm_conf	Set the image post processor
0xC0	set_lcd_gen0	Set the rise, fall, period and toggling properties of LCD signal generator 0
0xC1	get_lcd_gen0	Get the current settings of LCD signal generator 0
0xC2	set_lcd_gen1	Set the rise, fall, period and toggling properties of LCD signal generator 1
0xC3	get_lcd_gen1	Get the current settings of LCD signal generator 1
0xC4	set_lcd_gen2	Set the rise, fall, period and toggling properties of LCD signal generator 2
0xC5	get_lcd_gen2	Get the current settings of LCD signal generator 2
0xC6	set_lcd_gen3	Set the rise, fall, period and toggling properties of LCD signal generator 3
0xC7	get_lcd_gen3	Get the current settings of LCD signal generator 3
0xC8	set_gpio0_rop	Set the GPIO0 with respect to the LCD signal generators using ROP operation. No effect if the GPIO0 is configured as general GPIO.
0xC9	get_gpio0_rop	Get the GPIO0 properties with respect to the LCD signal generators.
0xCA	set_gpio1_rop	Set the GPIO1 with respect to the LCD signal generators using ROP operation. No effect if the GPIO1 is configured as general GPIO.
0xCB	get_gpio1_rop	Get the GPIO1 properties with respect to the LCD signal generators.
0xCC	set_gpio2_rop	Set the GPIO2 with respect to the LCD signal generators using ROP operation. No effect if the GPIO2 is configured as general GPIO.
Hex Code	Command	Description
0xCD	get_gpio2_rop	Get the GPIO2 properties with respect to the LCD signal generators.
0xCE	set_gpio3_rop	Set the GPIO3 with respect to the LCD signal generators using ROP operation. No effect if the GPIO3 is configured as general GPIO.
0xCF	get_gpio3_rop	Get the GPIO3 properties with respect to the LCD signal generators.
0xD0	set_dbc_conf	Set the dynamic back light configuration
0xD1	get_dbc_conf	Get the current dynamic back light configuration
0xD4	set_dbc_th	Set the threshold for each level of power saving
0xD5	get_dbc_th	Get the threshold for each level of power saving
0xE0	set_pll	Start the PLL. Before the start, the system was operated with the crystal oscillator or clock input
0xE2	set_pll_mn	Set the PLL
0xE3	get_pll_mn	Get the PLL settings
0xE4	get_pll_status	Get the current PLL status
0xE5	set_deep_sleep	Set deep sleep mode
0xE6	set_lshift_freq	Set the LSHIFT (pixel clock) frequency
0xE7	get_lshift_freq	Get current LSHIFT (pixel clock) frequency setting
0xE8	Reserved	Reserved
0xE9	Reserved	Reserved
0xF0	set_pixel_data_interface	Set the pixel data format of the parallel host processor interface
0xF1	get_pixel_data_interface	Get the current pixel data format settings
0xFF	Reserved	Reserved

Note. Please Refer to SSD1963 datasheet for details.

## 8.1.6 Hardware Related Parameter

### Booster and Power circuit

Internal DC-DC booster and Backlight driver are controlled by SSD1963 GPIO0 and GPIO1 respectively. It is necessary to enable them for normal operation via command

### Backlight Brightness PWM control

It is suggested to config the backlight brightness control signal as 3kHz PWM signal for best performance.

## 8.1.7 Startup Program (Example)

```

_RST=1; delays(10); // wait for all power stable
_RST=0; delays(1); // reset pulse
_RST=1; delays(10); // wait till internal reset routine finish

SdCmd(0xe2); SdData(0x3B); SdData(0x02); SdData(0x04); delays(10); // config PLL to 200MHz
SdCmd(0xe0); SdData(0x01); delays(10); // enable PLL
SdCmd(0xe0); SdData(0x03); delays(10); // switch to use PLL clock

SdCmd(0x11); // exit_sleep_mode
SdCmd(0x13); // enter_normal_mode (exit_partial_mode)
SdCmd(0x20); // exit_invert_mode
SdCmd(0x38); // exit_idle_mode (using full color)

SdCmd(0xB8); // set_gpio_conf
SdData(0x0f); // GPIO[0~3] controlled by host
SdData(0x01); // GPIO0 as normal GPIO
SdCmd(0xba); SdData(0x01); delays(10); // GPIO[0~3]=0001, enable DC-CD booster
SdCmd(0xba); SdData(0x03); delays(10); // GPIO[0~3]=0011, enable backlight booster

SdCmd(0xf0); SdData(0x00); // set_pixel_data_interface (MCU) 8bit
SdCmd(0xb0); // set_lcd_mode
SdData(0x24); // 24bit, disable FRC or dithering, DCLK=rising edge
SdData(0x20); // HSYNC=active lo, VSYNC=active low, default TFT m
SdData(0x02); SdData(0x7f); // panel size 640-1
SdData(0x01); SdData(0xdf); // panel size 480-1

SdCmd(0xb4); // set_hori_period
SdData(0x03); SdData(0x1f); // total pluse per line, HT=800-1
SdData(0x00); SdData(0x9f); // horizontal front porch, HPS=160-1
SdData(0x07); // HPW=0x07(default), not use
SdData(0x00); SdData(0x00); // LPS=0x0000(default), not use
SdData(0x00); // LPSPP=0x00(default), not use

SdCmd(0xb6); // set_vert_period
SdData(0x02); SdData(0x0c); // total line per frame, VT=525-1
SdData(0x00); SdData(0x2c); // vertical front porch, VPS=45-1
SdData(0x01); // VPW=0x01(default), not use
SdData(0x00); SdData(0x00); // FPS=0x0000(default), not use

SdCmd(0xe6); SdData(0x01); SdData(0xe0); SdData(0x00); // config PCLK=40ns(PLL@200MHz)

SdCmd(0x36); // set_address_mode
SdData(0x00); // top to bottom, left to right, RGB, normal

SdCmd(0xbe); // set_pwm_conf
SdData(0x00); // PWM clock set to 3kHz (PLL@200MHz)
SdData(150); // PWM width at about 60% (150/255)
SdData(0x01); // C[3]=0, non_DBC control; C[0]=1, enable PWM
SdData(0xf0); // DBC manual level at middle
SdData(0x00); // DBC minimum lever at middle
SdData(0x00); // disable the DBC response delay setting

SdCmd(0x29); // display on

SdCmd(0x2c); // write_memory_start
SdData(0xff); SdData(0xff); SdData(0xff); // write a white pixel
SdData(0xff); SdData(0x00); SdData(0x00); // write a red pixel
..... // continue writ display data

```

Note. Above example program may need modification to fit correspondent application.

## 9. Precautions of using LCD Modules

### Mounting

- Mounting must use holes arranged in four corners or four sides.
- The mounting structure so provide even force on to LCD module. Uneven force (ex. Twisted stress) should not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- It is suggested to attach a transparent protective plate to the surface in order to protect the polarizer. It should have sufficient strength in order to the resist external force.
- The housing should adopt radiation structure to satisfy the temperature specification.
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. Never rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics deteriorate the polarizer.)
- When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer

### Operating

- The spike noise causes the mis-operation of circuits. It should be within the  $\pm 200\text{mV}$  level (Over and under shoot voltage)
- Response time depends on the temperature.(In lower temperature, it becomes longer.)
- Brightness depends on the temperature. (In lower temperature, it becomes lower.) And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
- Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
- When fixed patterns are displayed for a long time, remnant image is likely to occur.
- Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference

### Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

### Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

### Storage

When storing modules as spares for a long time, the following precautions are necessary.

- Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between  $5^{\circ}\text{C}$  and  $35^{\circ}\text{C}$  at normal humidity.
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

### Protection Film

- When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
- The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to be main on the polarizer. Please carefully peel off the protection film without rubbing it against the polarizer.
- When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
- You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

### Transportation

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

**10. Appendix <Inspection items and criteria for appearance defect>**

**Bright/Dark Dots:**

Defect Type	Specification	Major	Minor
Bright Dots	$N \leq 2$		•
Dark Dots	$N \leq 3$		•
Total Bright and Dark Dots	$N \leq 4$		•

Note: 1. **The definition of dot:** The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.

2. **Bright dot:** Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.
3. **Dark dot:** Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.